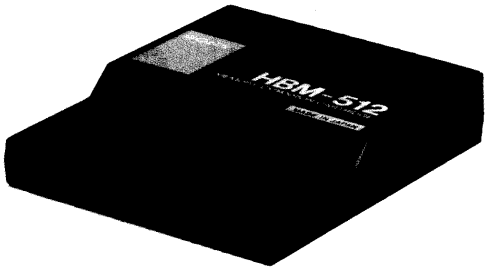
HBM-512

SERVICE MANUAL

AEP Model
UK Model



SPECIFICATIONS

Memory	512K byte
Power consumption	+5 V, 300 mA
Operating temperature and humidity	5° to 35°C (41°F to 95°F), 25% to 80%
Dimensions	Approx. 109 × 132 × 26.4 (w/h/d) ($4\frac{3}{8} \times 5\frac{3}{4} \times 1\frac{1}{16}$ inches)
Weight	Approx. 270 g (9.5 oz)

Design and specifications subject to change without notice.

MICROFILM

MEMORY EXPANSION CARTRIDGE

SONY®

ACC

SECTION 1
CIRCUIT DESCRIPTION

The HBM-512 is an expansion memory cartridge which is used for the HB-G900 MSX home computer. The RAM capacity is 512 k byts, as indicated by model name "512". The memory capacity of 512 k bytes is obtained by RAM chips IC16 through IC19. When using an exclusive program, this enables the expansion memory cartridge to be used as a large file which is almost the same as one floppy disk (512 k bytes). The RAM package can be used as a high-speed file because there is no mechanical access.

- **RAM TC514-256-12**

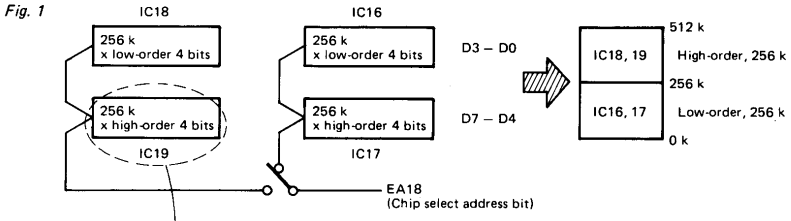
TC-514-256-12 has a memory capacity of 256 k x 4 bits and a high-speed access time of 120 nsec, as indicated by model names "256" and "–12". This RAM chip has four-bit (half-byte) data buses, and two stacked TC514-256-12s are used as eight bits (one byte). The four RAMs thus provide a capacity of 512 k bytes. TC514-256-12 is also a dynamic RAM with RAS ans CAS pins. It reads addresses A0 through A8 (adaptable in the 128-k-byte range) two times, then reads addresses A0 through A17 (adaptable in the 256-k-byte range) with the address doubled.

- **RAM Division**

CPU Z-80 can directly handle 64 k bytes by using its own address buses (A0 through A15). However, it cannot access over 64 k bytes. Therefore, the 512-k-byte RAM is divided as shown in the figures.

RAM Division

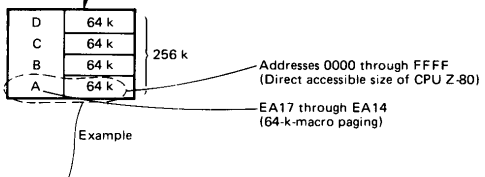
Fig. 1



Example

(256/64k)

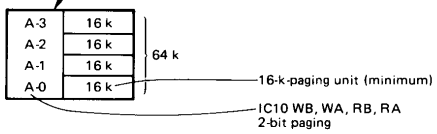
Fig. 2



Example

64k/16k)

Fig. 3



As shown in the figures above, the 512-k-byte RAM area is divided into minimum paging units of 16 k bytes, and each 16-k-byte unit is divided into 512/16 = 32 pages. The RAM's minimum page is not prescribed as 64 k bytes (CPU Z-80's access range) but as 16 k bytes because 64 k bytes are divided into four pages ("0" to "3") according to the MSX specification.

- **I/O Port and 16-k-byte Paging Circuit**

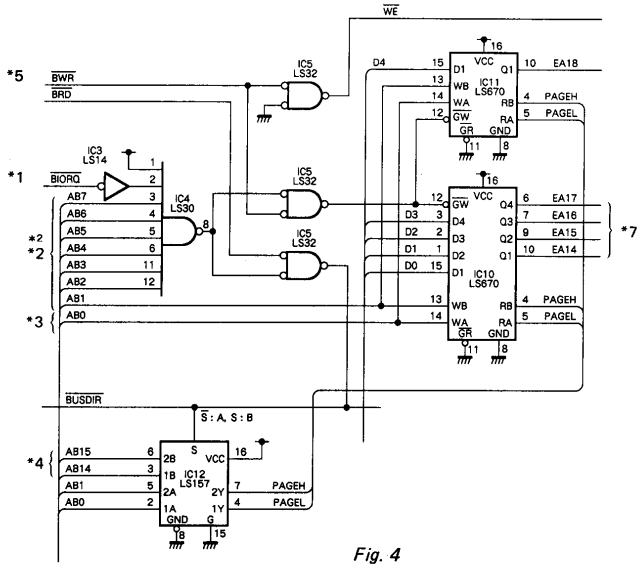


Fig. 4

- **Internal Configuration of IC10 and IC11**

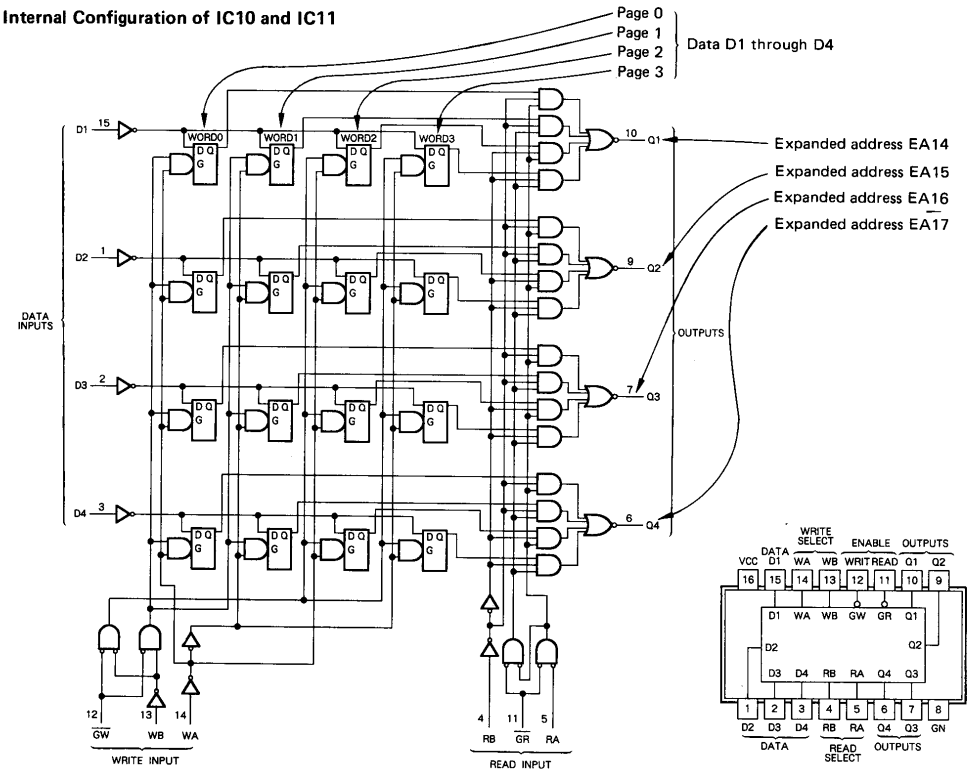


Fig. 5

Fig. 6

- **16-k-byte Paging**

When a pair of 256-k-byte RAMs is divided into 16-k-byte units, 256k/16k = 16 pages are obtained. In other words, the 256-k-byte RAM is divided into pages 0 through 15, arbitrary pages are picked up, and a continuous area of 64 k bytes is then formed. When the 64-k-byte area is formed, no overlapped page is used.

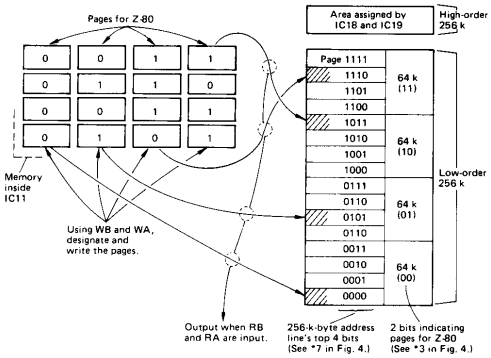


Fig. 7

As shown in Fig. 7, four arbitrary 16-k-byte areas are designated from the 256-k-byte RAM to make an access as a 64-k-byte RAM.

CPU Z-80 writes XXXX0000 into I/O port FC.
CPU-Z-80 writes XXXX0101 into I/O port FD.
CPU Z-80 writes XXXX1110 into I/O port FE.
CPU Z-80 writes XXXX1011 into I/O port FF.

At that time, the page number obtained when the 256 k bytes are divided by 16 is memorized in IC11 as shown in Fig. 7. This allows access to be mapped.

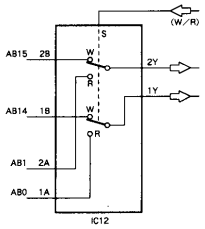
The above operation is done using the following:

I/O PORT: *1 ($\overline{\text{BIORQ}}$)
FC PORT: *2 (111111) and *3 (00)
WRITE: *5 ($\overline{\text{BWR}}$)
DATA BUS XXXX0000

Next, assume that CPU Z-80 writes "FF" into address 0002 (16). Address 0002 (16) is represented as 0000 0000 0000 0010 by an address bit. For a 16-k-byte page, for example, the address is represented by 14 bits (A13 through A0). This is based on the following:

16 bits (A15 through A0) = 64 k bytes
64 k bytes/4 = 16 k bytes

* Four can be represented in hexadecimal notation by two bits.



RA and RB select bits

Fig. 8

IC12 (LS157) is thus used, and the A14 and A15 signals (indicated by *4) are input to the PAGE select circuit as shown in Fig. 4. As a result, CPU Z-80 writes data by judging that 64 k bytes are divided into arbitrary 16-k-byte units. Any one of 16-k-byte pages 0 through F is actually substituted according to the signal output from IC11.

When "FF" is written into address 0002 (16), the "FF" is written into the third byte of 256-k-byte RAM's page 0000. Therefore, the area of 64 k bytes from the CPU can be freely set in 256 k bytes.

- **COLUMN/ROW (RAS, CAS) Select Circuit**

Address buses A0 through A18 are provided for the RAM. The 19 address inputs are sent to AB0 through AB13 and EA14 through EA17.

The select circuit used to send the output from AB0 through AB13 and EA14 through EA17 to RAM addresses A0 through A8 as COLUMN/ROW addresses is shown in Fig. 9.

The CPU generates addresses, and an $\overline{\text{SLTSL}}$ signal selects the cartridge. At that time, the ROW addresses are being determined.

First, assume that the EA18 signal for RAM chip selection is ignored. The $\overline{\text{SLTSL}}$ signal is passed through inverters two times. It then becomes an $\overline{\text{RASO}}$ signal and is sent to the $\overline{\text{RAS}}$ terminal.

The $\overline{\text{SEL}}$ signals at pin 1 of IC13, IC14, and IC15 are low at the trailing edge of the $\overline{\text{RAS}}$ signal. Therefore, the Y terminal of IC13, IC14, and IC15 is connected to AB0 through AB8 (ROW). The ROW addresses are sent to RAM.

When the clock goes from low to high during the positive period, Q (indicated by *1) of flip-flop IC6 (the $\overline{\text{SEL}}$ signal) goes high. The Y terminals of IC13, IC14, and IC15 are then set to the COLUMN position of AB9 through EA17.

When the $\overline{\text{SEL}}$ signals of IC13, IC14, and IC15 go high, the data is sent to the flip-flop (indicated by *2) at the trailing edge of the next clock pulse.

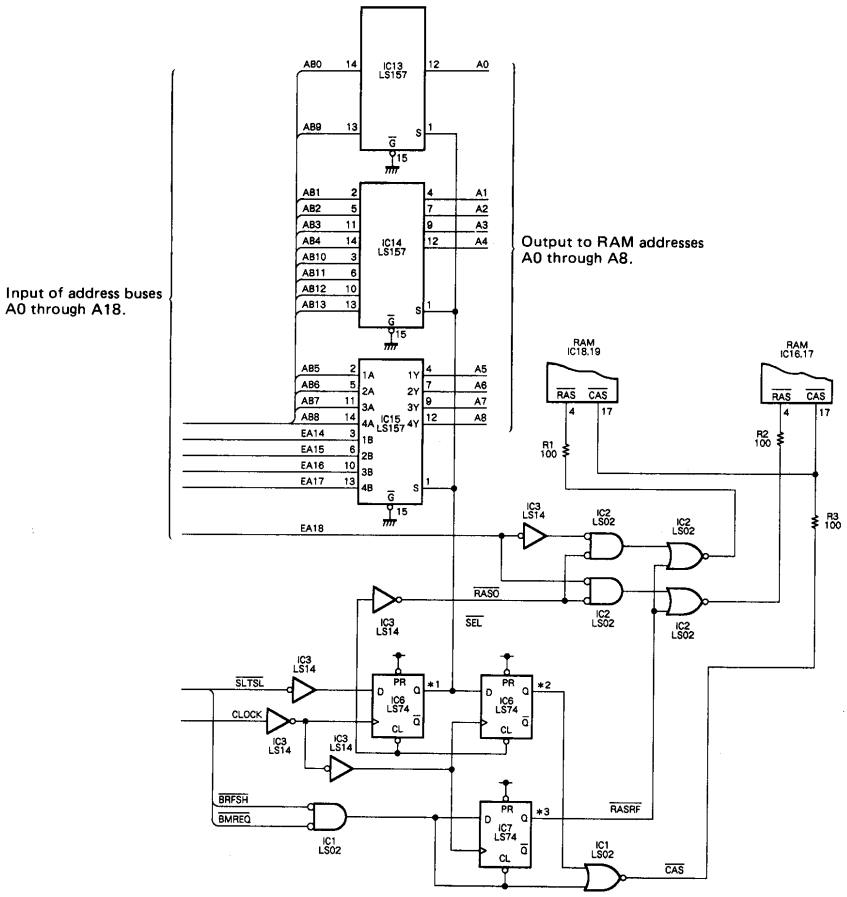


Fig. 9

When the refresh is not ignored, the output ($\overline{CAS}$) of IC1 goes low (that is, COLUMN period). The COLUMN address is memorized on the RAM during the COLUMN period. This operation is shown in Fig. 10.

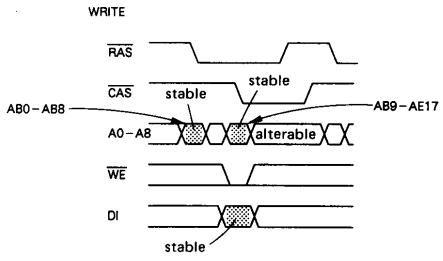


Fig. 10

EA18 is used to divide the RAM into two groups, upper and lower.

A $\overline{BRFSH}$ (buffered refresh) signal is generated at intervals of a few milliseconds to refresh and read the RAM. The resultant signal is branched into two routes and mixed with RAS and CAS signals.

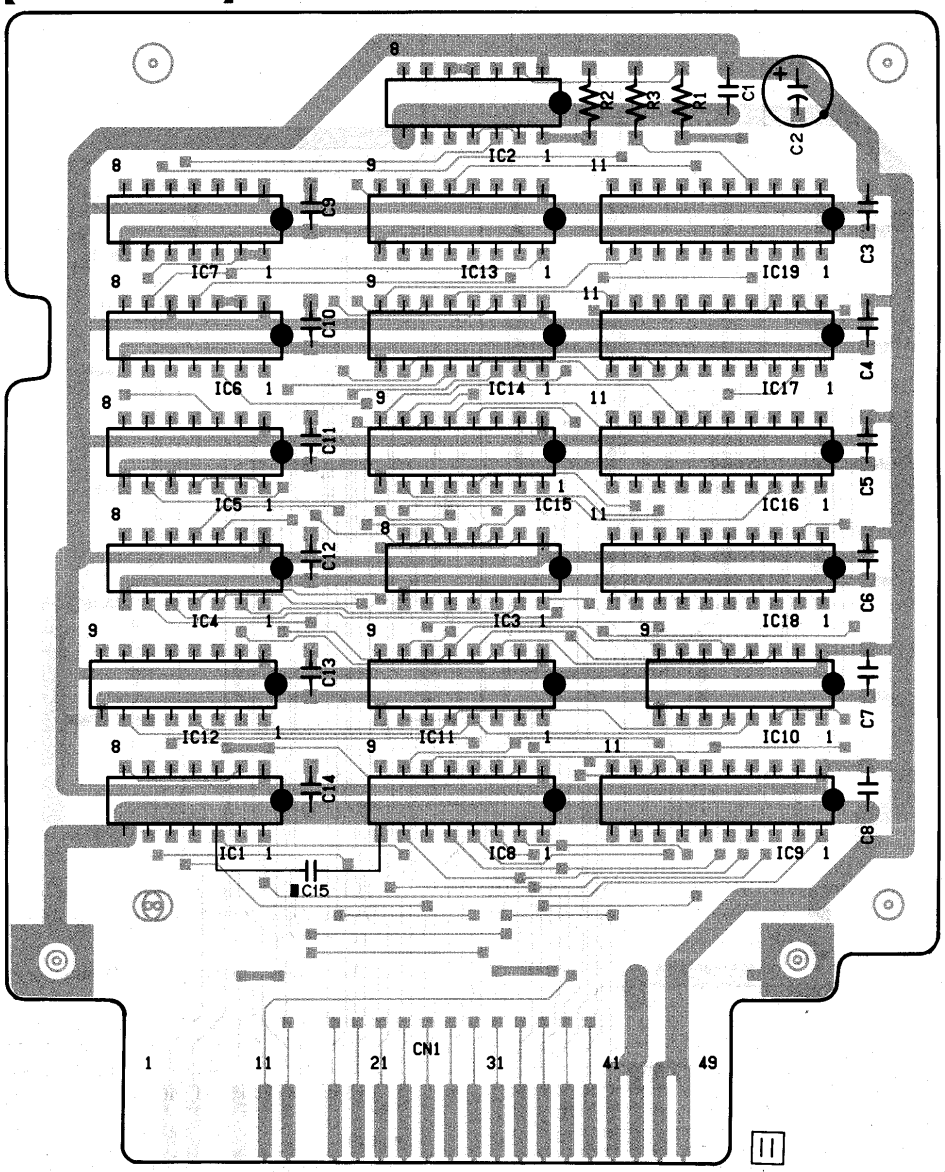
- **IC9**

This is a bidirectional buffer for data bus.
The description is omitted.

SECTION 2
DIAGRAMS

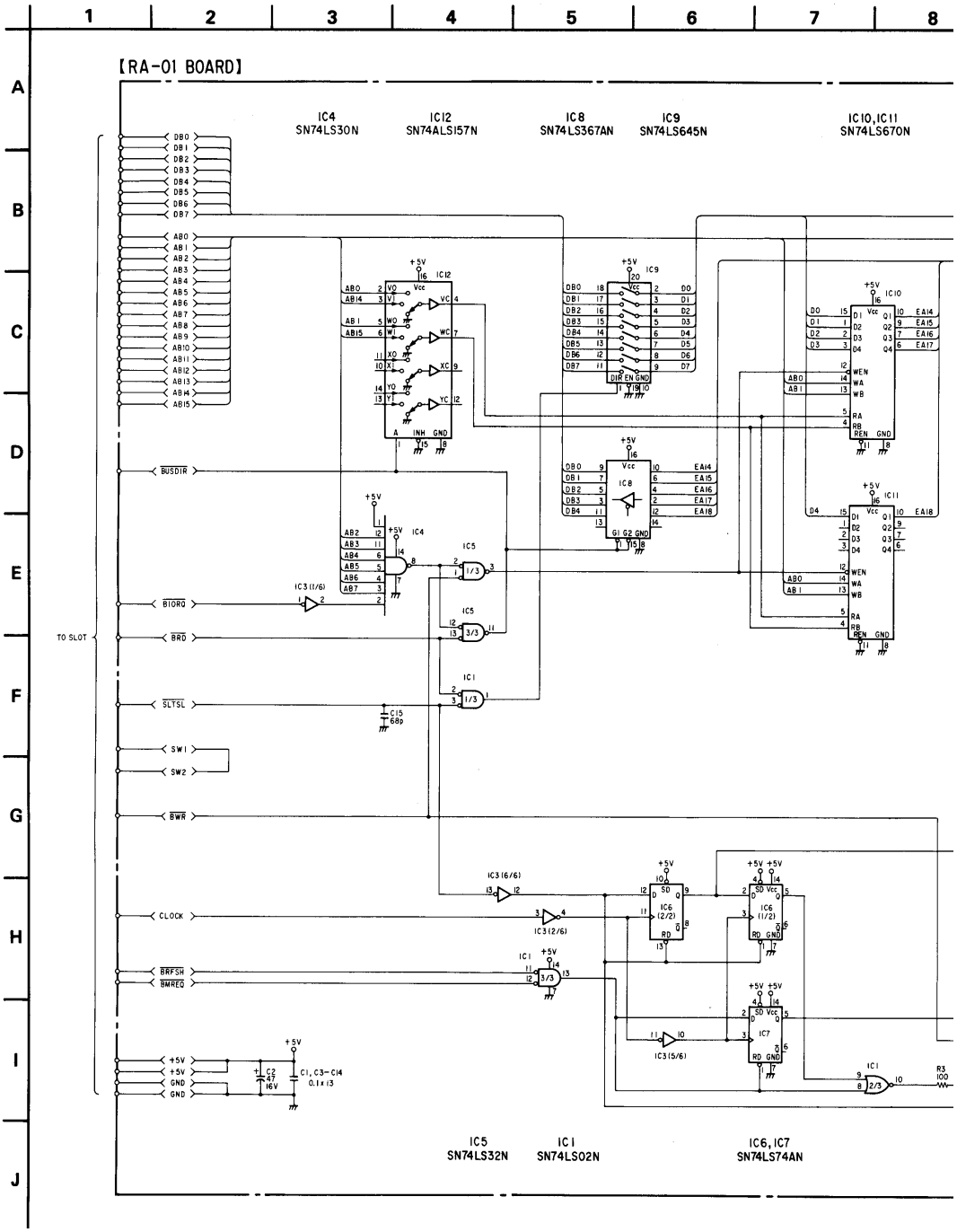
2-1. MOUNTING DIAGRAM

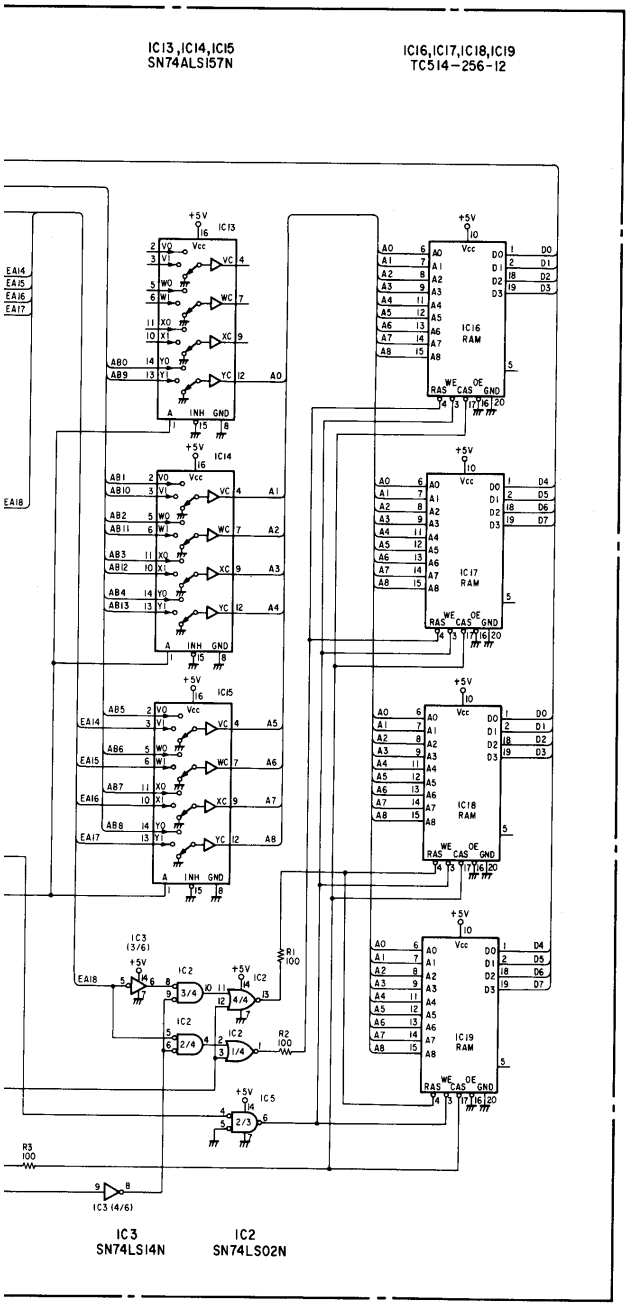
【RA-01 BOARD】



Note:

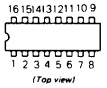
: component-side pattern.


1
2
3
4
5
6
7
8
A
B
C
D
E
F
G
H
I
J
【RA-01 BOARD】
IC4
SN74LS30N
IC12
SN74ALS157N
IC8
SN74LS367AN
IC9
SN74LS645N
IC10,IC11
SN74LS670N
IC5
SN74LS32N
IC1
SN74LS02N
IC6, IC7
SN74LS74AN
TO SLOT
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
AB14
AB15
BUSDIR
BIORQ
BRD
SLTSL
SW1
SW2
BWR
CLOCK
BRFSH
BMREQ
+5V
GND
C15
68p
C1, C3~C14
0.1x13
C2
47
16V
R3
100



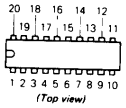
- **Semiconductor Lead Layouts**

SN74ALS157N
SN74LS367AN
SN74LS670N



SN74LS02N
SN74LS14N
SN74LS30N
SN74LS32N
SN74LS74AN

SN74LS645N



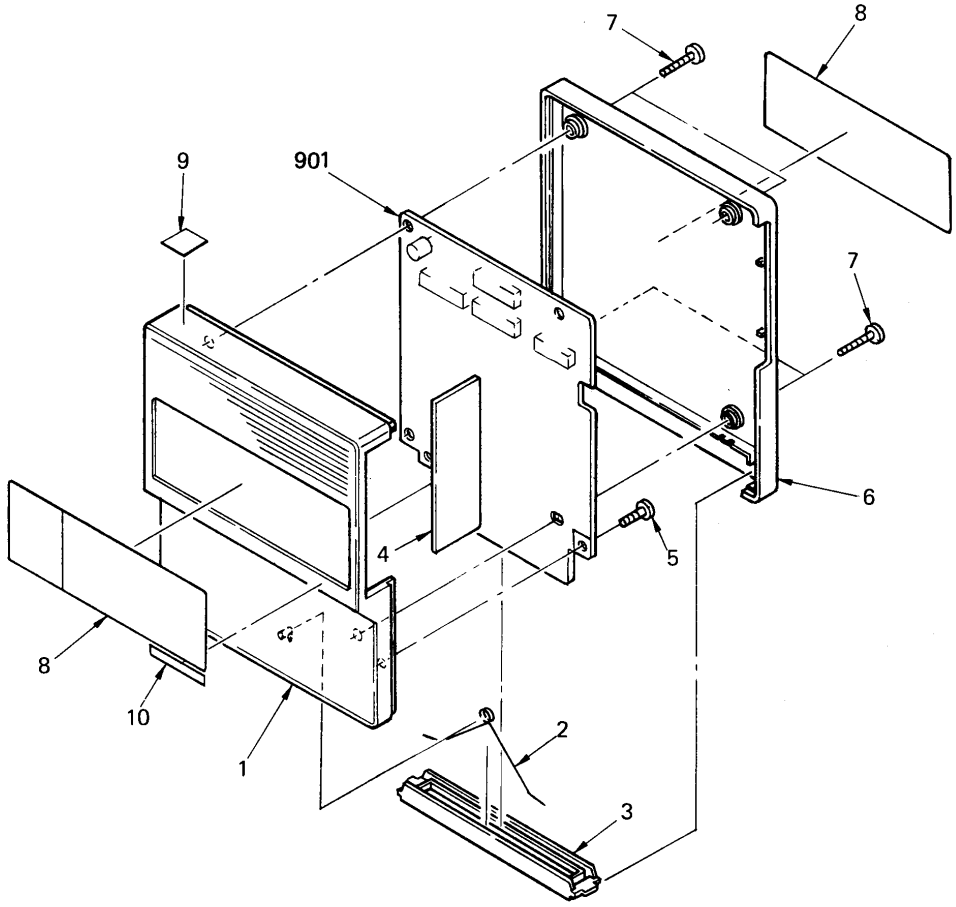
Note:

- All capacitors are in μF unless otherwise noted. pF: μμF 50WV or less are not indicated except for electrolytics and tantalums.
- All resistors are in Ω and ¼ W or less unless otherwise specified.

SECTION 3
EXPLODED VIEWS AND PARTS LIST

NOTE:

- The mechanical parts with no reference number in the exploded views are not supplied.
- Items marked " ★ " are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
- The construction parts of an assembled part are indicated with a collation number in the remark column.



No.	Part No.	Description	Remarks
1	4-606-570-02	CASE (FRONT), CARTRIDGE	
2	4-606-568-01	SPRING, TORSION	
3	4-606-567-02	PROTECTOR	
4	*4-612-050-01	COVER, PLATE	
5	7-685-133-19	SCREW +BTP 2.6X6 TYPE2 N-S	
6	4-606-569-02	CASE (REAR), CARTRIDGE	
7	7-685-536-19	SCREW +BTP 2.6X12 TYPE2 N-S	
8	*4-612-062-01	LABEL, CARTRIDGE	
9	3-703-713-01	STICKER, SONY SYMBOL (10)	
10	3-701-690-00	LABEL (MADE IN JAPAN)	
901	1-622-470-11	PC BOARD, RA-01	

SERVICE MANUAL

AEP Model
UK Model
No. 1

SUPPLEMENT

File this supplement with the service manual.

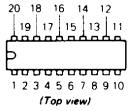
- Add the following component to the electrical parts list (page 10) and the semiconductor lead layouts (page 8) on the service manual.

1) Electrical Parts List (Page 10)

IC16–19 8-759-209-01 IC TC514256P-12

2) Semiconductor Lead Layouts (Page 8)

SN74LS645N
TC514256P-12



MEMORY EXPANSION CARTRIGE

SONY®

9-952-720-81

Sony Corporation
Audio Group

ACC

English
87E0537-1
Printed in Japan