# Service Manual <br> Personal Computer <br> $[\mathrm{GX}$ 




Design and Specifications are subject to change without notice.

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identifying the terminals in your plug, proceed as follows:

- The wire which is coloured blue must be connected to the terminal which is marked with the letter N or coloured black.
-The wire which is coloured brown must be connected to the terminal which is marked with the letter $L$ or coloured red.
Notes:
- Disconnect the mains plug from the supply socket when not in use. - Do not remove cover. Live parts inside.


## Location of Controls and Components



Rear View

(14) Sound output jack
(1) Function keys

Key used for easy inputs of predefined character strings.
(2) Power indicator

Lights when the power switch is turned on and goes out when the power is turned off.
(3) Special keys

Keys used to select, correct, and edit input characters, and control program execution.
(4) Space bar

Bar used to input a space between characters.
(5) Character keys

Keys used to input characters.
(6) Cursor keys

Keys used to move the cursor.
(7) (8) General port 1, General port 2 Connectors used to connect joysticks, tablets, etc.
(9) (10) Slot 1. Slot 2

Slots for MSX cartridges.
(11) Printer connector

Connector used to connect a printer, plotter, etc.
(12) Cassette Input/Output Connector Connector used to connect a cassette tape recorder.
(14) Sound output jack

Audio (sound) signal output jack. Connects to the TV audio input terminal.
(15) Video output jack

Video signal output jack. Connects to the TV video input terminal.
(16) RF output jack

RF signal output jack. Connects to the TV antenna terminal.
(17) Channel adjust trimmer After connecting the TV and computer, turn on the power switch. Set the TV to UHF channels 35-37. Insert the adjustment screwdriver into the channel adjust trimmer and adjust for a clear picture.
(18) Power switch

Power turns on when set to "ON" and the power indicator lights up. Power turns off when set to "OFF".
(13) Power cord

Memory Map (when using BASIC)
Address in hexadecimal


Area storing the program to which line numbers have been added.
Area for variables. For character variables, this area stores the pointer which points to the character string (string descriptor).
Area for array variables. If the array variables are of the character type, this area stores the pointer which points to the string in the string area. This area is allocated when the DIM statement is executed and an array with a subscript of 10 or less is used. The free area is an unused area. The size of the free area is the size of the user area minus the sizes of the character area, stack area, variable area, and program area. The size of the free area can be obtained by the FRE function.
Stack area storing the return address for BASIC when the FOR-NEXT statement or GOSUB statement is executed.
Area storing the strings contained in the character variables and array variables. The size of the string area is as specified in the CLEAR statement. If no size is specified in the CLEAR statement, an area of 200 bytes is allocated.
Area used during the input and output of files. This area is allocated according to the number specified in the MAXFILES statement.
The high limit address can be set in the CLEAR statement to F 380 or below so that an area (such as for machine language subroutines) can be allocated up until the work area for free use by the user.

## I/O Map

PPI (8255) Bit Assignment

| Port | Bit | I/0 | Signal Name | Description |
| :---: | :---: | :---: | :---: | :---: |
| A | $\begin{aligned} & 0 \\ & 1 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { CSOL } \\ & \text { CSOH } \end{aligned}$ | Specifies the slot number for addresses $\& H 0-\& H 3 F F$ |
|  | $\begin{aligned} & 2 \\ & 3 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { CS1L } \\ & \text { CS1H } \\ & \hline \end{aligned}$ | Specifies the slot number for addresses \&H4000- $\& \mathrm{H} 7 \mathrm{FFF}$ |
|  | $\begin{aligned} & 4 \\ & 5 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mathrm{CS} 2 \mathrm{~L} \\ & \mathrm{CS} 2 \mathrm{H} \\ & \hline \end{aligned}$ | Specifies the slot number for addresses \&H8000-\&H8FFF |
|  | $\begin{aligned} & 6 \\ & 7 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { CS3L } \\ & \text { CS3H } \\ & \hline \end{aligned}$ | Specifies the slot number for addresses \&HCOOO-\&HFFFF |
| B | 0 7 7 | Input |  | Keyboard return signal |
| C | $\begin{array}{ll} \hline 0, & 1 \\ 2, & 3 \\ \hline \end{array}$ |  | $\begin{array}{ll} \hline \text { KB0, } & \text { KB1 } \\ \text { KB2, } & \text { KB3 } \\ \hline \end{array}$ | Keyboard scan signal |
|  | 4 |  | CASON | Cassette control (ON when L) |
|  | 5 |  | CASW | Cassette write signal |
|  | 6 |  | CAPS | CAPS lamp signal (lights when L) |
|  | 7 |  | SOUND | Software controlled sound output |


e mark are provided to optional equipment. - For details on the VDP, PSG, and PPI, see their respective manuals. - Addresses $\& H 40-\& H F F$ represent the system reserve area.

PSG Bit Assignment

| Port | Bit | I/O | Bit 6 at Port B | Connector Pin Number |
| :---: | :---: | :---: | :---: | :---: |
| A | 0 | Input | Low level High level | Port 1 pin 1 <br> Port 2 pin 1 |
|  | 1 |  | Low level High level | Port 1 pin 2 <br> Port 2 pin 2 |
|  | 2 |  | Low level High level | Port 1 pin 3 <br> Port 2 pin 3 |
|  | 3 |  | Low level High level | Port 1 pin 4 Port 2 pin 4 |
|  | 4 |  | Low level High level | Port 1 pin 6 <br> Port 2 pin 6 |
|  | 5 |  | Low level High level | Port 1 pin 7 <br> Port 2 pin 7 |
|  | 6 |  | Keymatrix assignment input (low level) |  |
|  | 7 |  | CSAR (Read signal of the cassette tape) |  |
| B | 0 | Output | Port 1 pin 67 |  |
|  | 1 |  | Port 1 pin 7 Note 2 |  |
|  | 2 |  | Port 2 pin 6 |  |
|  | 3 |  | Port 2 pin 7 , |  |
|  | 4 |  | Port 1 pin 8 |  |
|  | 5 |  | Port 2 pin 8 |  |
|  | 6 |  | Input select of port $A$ |  |
|  | 7 |  | - |  |

Note 1: Either port 1 or 2 is selected by the output level of bit 6 at port $B$. Writing a "l" to bit 6 at port $B \rightarrow$ high level output $\rightarrow$ port 2 selected. Writing a " 0 " to bit 6 at port $B \rightarrow$ low level output $\rightarrow$ port 1 selected.
Note 2: Be sure to output a high level at these pins if port $B$ is to be used for input.

## General for Peripheral Circuit

## CPU (Central Processing Unit) Peripheral

 CircuitCPU Peripheral Circuit consists of CPU, Clock Generator Circuit and Reset Circuit.
Z80A ( $\mu$ PD780C-1, IC8) is used as CPU. An interruption system is maskable interrupt, not non-maskable. AND signals of VDP's $\overline{\mathrm{INT}}$ and an external interrupt are fed to $\overline{\text { INT }}$ terminal. In Ml cycle, 1 WAIT is inserted, and external WAIT is accepted asynchronously with CLOCK signal. $\overline{B U S R Q}$ and $\overline{B U S A K}$ are not used, neither DMA function.


Fig. 1 CPU Peripheral Circuit

The CLOCK Generator Circuit--Serial Oscillation Circuit of 74 HCO 4 (IC43)-oscillates 10.6781522 MHz to generate VDP CLOCK and, at the same time, generates CPU CLOCK in the circuit of 74LS74 (IC42) and 74 LS 107 (IC47) which divides VDP CLOCK by 3 to get 3.559384 MHz . Moreover, CLOCK Generator Circuit divides CPU CLOCK into halves to get 1.779462 MHz by 74LS74 (IC39) and generates PSG CLOCK.


Fig. 2 CLOCK Waveform
The Reset Circuit utilizes the charge of CR Circuit (C13 and R26), but it takes too much time to raise RESET signal by only the CR. So the circuit is compulsively raised by Q10, when each end of C becomes about 1.5 V . Therefore, RESET signal changes "L" into "H" in 60 ms after power source $O N$.


Fig. 3 RESET Signal
ROM R
This system uses 32 K x 8 bits MASK ROM (IC32, MN23257) which builds in the MSX BASIC. $\overline{\mathrm{CS}}$ is connected to SLTO, and $\overline{\mathrm{EE}}$ to Al5. Access time is available up to 325 ns .


Fig. 4 ROM Periphery

Main Memory Peripheral Circuit consists of Main Memory and Memory Access Circuit.
The Main Memory has a 64 KB memory space by using eight $16 \mathrm{~K} \times 8$-bit DRAMs. Refresh is performed by RAS-ONLY REFRESH. Because RAS pre-charge time in refreshing Ml cycle is ensured to be 100 ns by Timing Chart, the access time of RAM must be 150 ns. In the Memory Access Circuit, $\overline{R A S}$ is generated by $\overline{M E R Q}$ or RESH and CLOCK. The switchover of the row address to the column address is
done by the multiplexer 74LS157 and $\overline{\mathrm{CAS}}$ is generated by being staggered the time, with the condenser C35, when the column address is outputted. C35 ensures that the $\overline{C A S}$ will be "L", considering differences of the output timing of 74LS157, after the switchover of the row address to the column address.
$\overline{\mathrm{WE}}$ is generated by $\overline{\mathrm{BWR}}$, and $\overline{\mathrm{OE}}$ by $\overline{\mathrm{BRD}}$.
$\overline{R A S}, \overline{C A S}, \overline{W E}$ and $\overline{O E}$ protect from the undershoot by being inserted a resistance for the damping.


Fig. 5 I/O Select Peripheral Circuit

I/O Select Peripheral Circuit
All of Input/Output with external equipment are done through $I / 0$ ports in this system, and an access signal of each port is generated in this circuit. I/O Select Peripheral Circuit consists of I/O Select Generator Circuit, Chip Access Signal Generator Circuit and Short Write Generating Circuit.


Fig. 6 I/O Select Peripheral Circuit

I/O Select Generator Circuit generates I/O Select signal according to the I/O map. This signal is generated through high-order five bits in low-order byte of Address Bus and through BIORQ and Multiplexer 74LS138 (IC25). In order to ensure data stabilizing time when PSG is engaged in WRITE, and to be considered
that the output delay time is 350 ns when PPI is in WRITE, WRITE signal is raised faster by Short Write Generator Circuit.
Chip Access Generator Circuit generates $\overline{\mathrm{CSW}} / \overline{\mathrm{CSR}}$ (VDP Access signals), $\overline{\mathrm{PP} I W R /}$ PPIRD (PPI Access signals) and BCl/BDIR (PSG Access signals) from $I / O$ Select signal and $\overline{\mathrm{BWR}} / \overline{\mathrm{BRD}} / \overline{\mathrm{SWR}}$.

VDP (Video Display Processor) Peripheral Circuit

This system uses TI's TMS9929A as CRTC. This LSI's features are as follows.
. $256 \times 192$ pixels resolution
. Used 4,8 and 16 KB as VRAM ( 16 KB is used in MSX.)

- Automatic refreshing function of VRAM
- Composite video output, in PAL system
- Interruptible in every frame
- Automatic processing of the sprite screen.

|  | Resolution | Pattern <br> Size | Patterns | Colours | Sprite | Screen |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Graphic I <br> (SCREEN 1) | $192 \times 256$ <br> pixels | $8 \times 8$ <br> pixels | 256 <br> patterns | 16 <br> colours | usable | 24rows x 32columns |
| (768) |  |  |  |  |  |  |

Table 1 Screen Mode of VDP.

A VDP's operation depends on values of 9 registers in VDP and a table on VRAM. VDP has three control signals which are $\overline{\mathrm{CSW}}, \overline{\mathrm{CSR}}$ and MODE. MODE signal distinguishes which should be a candidate for

READ and WRITE, VDP resistor or VRAM. In "L", VRAM is the candidate. AO is connected to MODE terminal. $\overline{\operatorname{CS}} \bar{R}$ is generated by Inverted NAND of $\overline{C S V D P}$ and $\overline{\mathrm{RD}}$, and $\overline{\mathrm{CSW}}$ is by OR of $\overline{\mathrm{CSVDP}}$ and $\overline{\mathrm{WR}}$.


Fig. 7 VDP Peripheral Circuit Diagram

| PSG (Programmable Sound Generator) |
| :--- |
| Peripheral Circuit |

PSG Block consists of PSG and General Port Circuit. This system uses GI's AY-3-8910A as PSG, which makes it enable to produce 8 octaves, triple chords and noise-sound effects. This LSI builds in a tone generator, a noise generator, an envelope generator and 16 registers whose each value decides the frequency
and the volume of the sound by software. This LSI has also two I/O ports which are available for Input/Output with General Port, Keyboard Control and input to a cassette tape recorder. In this occasion, each bit in port $A / B$ is assigned as the following table.

| Signal | I/O | Function |
| :---: | :---: | :---: |
| IO A0 | Input | PORT 1-1 PORT 2-1 |
| IO Al |  | PORT 1-2 PORT 2-2 |
| IO A2 |  | PORT 1-3 PORT 2-3 |
| IO A3 |  | PORT 1-4 PORT 2-4 |
| I0 A4 |  | PORT 1-6 PORT 2-6 |
| IO A5 |  | PORT 1-7 PORT 2-7 |
| I0 A6 |  | Input specifying the layout of Keyboard |
| I0 A7 |  | Read signal input from a cassette tape recorder |
| IO B0 | Output | PORT1 |
| IO B1 |  | PORT1 |
| IO B2 |  | PORT2 |
| 10 B 3 |  | PORT2 |
| IO B4 |  | PORT1 |
| IO B5 |  | PORT2 |
| I0 B6 |  | Selecting input of PORT A "L"=PORT 1 " $\mathrm{H}^{\prime}=$ PORT 2 |
| I0 B7 |  | -_ |

Table 2 Bit-Assignment in PSG Port

PSG has three control lines--BDIR, BCl and $B C 2--$, whose control signals in

Input/Output are shown as the following table.

| BDIR | BC1 | BC2 | State |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | Not Selected |
| 0 | 1 | 1 | Readout from PSG |
| 1 | 0 | 1 | Writing in PSG |
| 1 | 1 | 1 | Address latch |

Table 3 PSG Control Signal

In General Port Circuit, there are two (IC28, 33) and open collector gate general ports (Input 4-bit, Output 1-bit and I/O 2-bit) using multiplexer 74LS157

74LS09 (IC37, 40).


Fig. 8 PSG Peripheral Circuit

CF-2700 uses AY-3-8910A whose maximum access time is 200 ns and minimum width of write data pulse is 165 ns .

| PPI (Programmable Peripheral Interface) <br> Peripheral Circuit |
| :--- |

PPI Block consists of PPI (using $\mu$ PD8255AC-5), Keyboard Control Circuit and Slot Signal Generator Circuit. CF-2700 adopts MODE 0 (ports A,C for output, and port $B$ for input). This LSI is utilized for specifying the slot num-

| Port | I/O | Bit | Function |
| :---: | :---: | :---: | :--- |
| A | Output | $0 \sim 7$ | Specifying the Slot Number |
| B | Input | $0 \sim 7$ | Keyboard Return Signal |
| C | Output | $0 \sim 3$ | Keyboard Scan Signal |
|  |  | 4 | Controlling the motor of a cassette tape recorder 0=0N 1=0FF |
|  |  | 5 | Signal writing in a cassette tape recorder |
|  |  | 6 | Controlling Keyboard CAPS Lamp 0=LIGHTING |
|  |  | 7 | Output of Click Sound |

Table 4 Port function in PPI


Fig. 9 PPI Peripheral Circuit
Port $A$ is used for specifying the slot number of address bank in units of 16 KB. Port A is preset for this operation as the following table.

| Bit of <br> Port A | Contents |
| :---: | :---: |
| PA1 PA0 | Slot Number of Page 0 |
| PA3 PA2 | Slot Number of Page 1 |
| PA5 PA4 | Slot Number of Page 2 |
| PA7 PA6 | Slot Number of Page 3 |

Table 5 Meaning of each bit in Port A
Keyboard Scan signals ( $0-3$ bits) of Port C are decoded by 74LS145 (IC46) and inputted to Port B through Keyboard.


Slot signal is generated from a signal which is set up in Port A by data selector 74LS153 (ICl0) and decoder 74LS139 (IC23).

## Cartridge

Signals connected to Cartridge Slot are described in the table 6 and explained in the table 7.
Data bus is connected via Buffer 74LS245 (IC5). When I/O or Slot 0 is selected, the mainframe and the slot are separated and the bus is controlled to go to the mainframe in READ and INTERRUPT operations.


Fig. 11 Data Bus/Buffer Circuit $\overline{\mathrm{CSI}}, \overline{\mathrm{CS} 2}$ and $\overline{\mathrm{CS} 12}$ are generated from Al5 and A14 by decoder 74LS139. (IC23).


Fig. 12 Chip Select Generator Circuit

Fig 10 Slot Signal Generator Circuit

| Pin <br> Number | Name | I/O <br> Note 1 | Pin <br> Number | Name | $I / 0$ <br> Note 1 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | $\overline{\mathrm{CSI}}$ | 0 | 2 | $\overline{\mathrm{CS} 2}$ | 0 |
| 3 | $\overline{\text { CS12 }}$ | 0 | 4 | SLTSL | 0 |
| 5 | RESERVED | - | 6 | $\overline{\mathrm{RFSH}}$ | 0 |
| 7 | WAIT | I | 8 | $\overline{\text { INT }}$ | I |
| 9 | MI | 0 | 10 | $\overline{\text { BUSDIR }}$ | I |
| 11 | $\overline{\text { IORQ }}$ | 0 | 12 | $\overline{\text { MERQ }}$ | 0 |
| 13 | $\overline{W R}$ | 0 | 14 | $\overline{\mathrm{RD}}$ | 0 |
| 15 | RESET | 0 | 16 | RESERVED | - |
| 17 | A9 | 0 | 18 | A15 | 0 |
| 19 | Al1 | 0 | 20 | A10 | 0 |
| 21 | A7 | 0 | 22 | A6 | 0 |
| 23 | Al2 | 0 | 24 | A8 | 0 |
| 25 | Al4 | 0 | 26 | Al3 | 0 |
| 27 | A1 | 0 | 28 | A0 | 0 |
| 29 | A3 | 0 | 30 | A2 | 0 |
| 31 | A5 | 0 | 32 | A4 | 0 |
| 33 | D1 | I/0 | 34 | D0 | I/0 |
| 35 | D3 | I/0 | 36 | D2 | I/O |
| 37 | D5 | I/0 | 38 | D4 | I/0 |
| 39 | D7 | I/0 | 40 | D6 | I/O |
| 41 | GND | - | 42 | CLOCK | 0 |
| 43 | GND | - | 44 | SW1 | - |
| 45 | +5V | - | 46 | SW2 | - |
| 47 | +5 V | - | 48 | +12 V | - |
| 49 | SUNDIN | I | 50 | $-12 \mathrm{~V}$ | - |

a) Note 1:The distinction of Input/Output is based on the mainframe. b) Reserved terminals are forbidden using.

Table $6 \quad \begin{aligned} & \text { Connected Signal Lines of } \\ & \text { Cartridge Bus }\end{aligned}$

| Pin No. | Name | Contents |
| :---: | :---: | :---: |
| 1 | CS1 | ROM 4000...7FFF Address Select Signal |
| 2 | CS2 | ROM 8000... BFFF Address Select Signal |
| 3 | CS12 | ROM 4000... BFFF Address Select Signal ( 256 K for ROM) |
| 4 | SLTSL | Slot Select Signal adds Select Signal peculiar to each slot |
| 5 | RESERVED | For Future use |
| 6 | RFSH | Refresh Cycle Signal |
| 7 | WAIT | WAIT Request Signal to CPU |
| 8 | INT | INTERRUPT Request Signal to CPU |
| 9 | M1 | CPU Fetch Cycle Signal |
| 10 | BUSDIR | Control Signal for direction of external Data Bus Select a cartridge and outputs $L$ level from each cartridge except Memory at the same time when the data are outputted. |
| 11 | IORQ | I/O Request Signal |
| 12 | MERQ | Memory Request Signal |
| 13 | WR | Write Timing Signal |
| 14 | RD | Read Timing Signal |
| 15 | RESET | System Reset Signal |
| 16 | RESERVED | For furture use |
| 17~32 | A0~A15 | Address Bus Signal |
| 33~40 | D0~D7 | Data Bus Signal |
| 41 | GND | Ground |
| 42 | CLOCK | CPU Clock 3.559 MHz |
| 43 | GND | Ground |
| 44,46 | SW1, SW2 | For protect in Connect/Disconnet |
| 45,47 | +5 V | Powr Source +5 V |
| 48 | +12 V | Power Source +12 V |
| 49 | SUNDIN | Sound Input Signal ( -5 dbm ) |
| 50 | -12 V | Power Source -12 V |

Table 7 Explanation of Signal Lines

Cassette Interface Circuit
MSX uses FSK method for recording, whose
2400 baud and the transfer waveform is transfer rate supports 1200 baud and shown in the table 8.

|  | 0 | 1 |
| :---: | :---: | :---: |
| 1200 baud |  |  |
| 2400 baud | $\square$ <br> 2400 Hz 1 Wave |  |

## Table 8 Data Waveform

Therefore, Interface Circuit must ensure $1200 \mathrm{~Hz}-4800 \mathrm{~Hz}$ transfer.
(i) Input Circuit


Fig. 13 Cassette Input Circuit
Input terminal is terminated by the 150 $\Omega$ resistance whose value is set for adjusting to the amplifier's characteristic on the cassette. This circuit has the gain by using OP-Amp. and also the characteristic as the filter, the waveform characteristic at this time is as follows.
This circuit uses a high-speed comparator to ensure the reproducing of 4800 Hz waveform. The standard voltage supplied to the comparator is set to about 2.5 V by resistance-division. This voltage is used in the bias voltage at the $\Theta$ terminal. R54 and R55 let the circuit have the hysteresis characteristic and increase the noise margin.


Fig. 14 Waveform Characteristic in Cassette Input Circuit


This circuit using the DROPPER system is to supply four kinds power of $+5 \mathrm{~V},-5 \mathrm{~V}$, +12 V and -12 V .
In a primary circuit, there is a line filter composed of condensers and coils that is to prevent a malfunction due to external noises and reduce useless radiation outward.
In a voltage-regulator circuit of a secondary circuit, +5 V circuit consists of discrete elements and $+12 \mathrm{~V},-5 \mathrm{~V},-12 \mathrm{~V}$ circuits are composed of general constant-voltage regulator ICs.
(1) Operation of +5 V Voltage-Regulator Circuit
A voltage that is rectified in full wave by diodes (D7, D8) and flattened by electrolytic capacitor (C7) is applied into a emitter (transistor Q1). The base current of the transistor Q1 is governed by a transistor Q7. The stabilization of the output voltage is achieved by varing the base current of the transistor Q1 that is to change Vce of Q1.

This circuit produces a required reference voltage by dividing +12 V constant-voltage output with resistances R5, VR1 and R80, that is, enables to vary an output voltage by adjusting a value of VR1 (voltagedividing ratio).
The detection of errors between the reference and output voltages is made in a differential amplification circuit of transistors Q8 and Q2. This control method is as the following.
(1) +5 V output voltage ascends.
(2) Base current of the transistor Q8 decreases.Current flowing into the resistance Rl decreases.
(4) Base current of the transistor Q7 decreases.
$\downarrow$
(5) Base current of the transistor Q1 decreases.

## $\downarrow$

(6) VCE of the transistor Q1 increase. $\downarrow$
(7) Output voltage descends.

When the output voltage descends, the contrary phenomena to the above happens--the VCE of the transistor Q1 decreases and the output voltage increases.
(2) Operation of +12 V Voltage-Regulator Circuit
A voltage that is rectified in full wave by diodes (D3, D5) and flattened by an electrolytic capacitor ClO is inputted into an input terminal of a regulator IC (IC1). This IC1, which is for the constantvoltage power supply, outputs stabilized +12 V into an output terminal. Moreover, this IC can control the output with an external signal, but we will describe it in details later.

(3) Operation of -12 V Voltage-Regulator Circuit
A voltage that is rectified in full wave by diodes (D4, D6) and flattened by an electrolytic capacitor C6 is inputted into an input terminal of a regulator IC (IC2). This IC2, which is for the constantvoltage power, outputs stabilized -12 V into an output terminal.
(4) Control of Output Voltage with External Signal
The PSW terminal can control the output of +5 V and +12 V . When the PSW terminal is connected with GND, each voltage is outputted normally, and when it is open each voltage becomes about $0 \mathrm{~V} .(-12 \mathrm{~V}$ and $-5 \mathrm{~V}$ are left as it is.)

This control is made by transistor Q9 and ICl. Pin No. 4 in ICl is a terminal of which output voltage becomes about 0 V when current more than about $500 \mu \mathrm{~A}$ flows. If controlled this pin externally, it enables to control +12 V output voltage. The +5 V output is to be 0 V with +12 V being 0 V , because its reference voltage is made by dividing +12 V , as described in (1).

The output voltage control by the Pin No. 4 in ICl is as the following.
(1) PSW terminal is connected with GND.
(2) Transistor Q9 is cut off.
(3) Current of Pin No. 4 in ICl is near about 0 V .

## $\downarrow$

(4) Output voltage of ICI is +12 V .

SW terminal in open:
(1) PSW terminal is opened.
(2) Transistor Q9 is on.
(3) Current of Pin No. 4 in ICl flows. $\downarrow$
(4) Output voltage of IC1 is about 0 V .

R38 and C38 compose of a time constant circuit that delays rising +5 V and +12 V. R37 is a resistance for an electric discharge of C38.

## Display Screen

Note the following points for an easy to see screen.

- Depending on the type of TV, the left and right edges may not be displayed on the TV screen. This may result because the display area of the TV and that of the personal computer are different. If this is the case, do not use the shaded part shown in the illustration. In the text mode, set the displayed columns using the WIDTH command to 28-29 (see the "MSX-BASIC manual"). (It is preset to 37 columns when the power is turned on.) In the graphic mode, do not use the $10-16$ dots on the left and right sides when writing a program.


32 -column text mode



This part is cut off.
40-column text mode

- Do not adjust the screen any brighter than necessary.
- Exercise care in combining colors when programming. The screen may be hard to read due to blurred colors depending on the combination of the foreground color (color of characters, etc.) and the background color. White on blue (Color 15, 5) is a relatively easy to distinguish combination. (Color 25, 4, 4 is set when the power is turned on.)
- The color and volume settings on the TV for personal computer use are slightly different from that for TV broadcast reception. Adjust according$1 y$ when switching from a TV broadcast to the personal computer.
Note 1: Character patterns are displayed as $8 \mathrm{H} \times 6 \mathrm{~W}$ dots/character in the 40-column text display mode (SCREEN 0). ( 8 H x 8 W dots/character in the $32-$ column text display mode.) For this reason, the right side of some graphic symbols may be cut off when displayed. (Letters and numbers are always displayed as full characters.)


## Character Codes



Examples: The character code for $A$ is $\& H 41=16 \times 4+1=65$ (Decimal)

## Input and output of Graphic Symbols

Graphic symbols are input and output by adding a graphic header (\&HOl).
For example, to input and output "O" the graphic header is used as follows. Input from the keyboard: Two bytes, \&HOl and $\& \mathrm{H} 4 \mathrm{~A}$, are input.
Output to the TV or printer: Two bytes, \&HO1 and \&H4A, are output.
Example: To output to a TV:
PRINT CHR\$ (1); CHR\$ (\&H4A);

Reference: Correspondence between decimal and hexadecimal numbers.

| Decimal | $0 \sim 9$ | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | $\ldots$ | 31 | 32 | 33 | $\ldots$ | 63 | 64 | $\ldots$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 255 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Hexadecimal | $0 \sim 9$ | A | B | C | D | E | F | 10 | 11 | 12 | $\ldots$ | 1 F | 20 | 21 | $\ldots$ | $3 F$ | 40 | $\ldots$ |
| FF |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

In other words, $X_{2} X_{1}$ (hexadecimal)

$$
=x_{2} \times 16+X_{1} \quad(\text { decimal })
$$

Examples: $\& H 1 F=1 x 16+15=31$ (decima1) $\& H F F=15 \times 16+15=255$ (decima1)

## Self Test

## 1. Outline of Self Test

This Self Test Program is prepared for the purpose of testing hardware functions of Personal Computer CF-2700. This program is to start at the 8000 H address and materials in 16 KB ROM is supplied through the slot.

## 2. Self Test Program

This program is made up of two main CHECK parts.

1) The first CHECK part-- forbasic checks.
(1) Check the diagnostic program on. Make sure that this program is started correctly.
(2) VDP/VRAM basic check

Check if the interrupt flag is correctly set or reset (between CPU - VPD), and the Read/Write of VRAM (CPU - VDP - VRAM) is done correctly.
(3) Printer basic check

Check if the printer is connected properly and can print out checked results.
(4) RAM check Check if data are correctly written in a specified address.
(5) PSG check

Check if the Read/Write of PSG register (CPU - PSG) and the data input/output of $I / O$ port (PSG PSG) are made correctly.
(6) Key input check Check if the key input works correctly.
2) The second CHECK part -- for checks including external peripheral equipment.
(7) ROM check

Check if the interpreter operates correctly.
(8) Screen display check

Check if the screen displays correctly.
(9) Cassette I/O check

Check if signals are inputted/ outputted correctly.
(10) Joystick input check

Check if the joystick sends its
signals correctly by operating it.
(11) Print out check

Check if the printer is sent the correct print out data.
(12) Audio output check

Check if the audio sound is outputted properly.
3. Self Test Procedure

1) Equipment required
(1) Test Personal Computer,

Model No.: CF-2700............. 1 unit
(2) Printer or Plotter
(designed for MSX)............. 1 unit
(3) Joystick

Model No.: CF-2201............. 1 unit
2) Connection of Equipment

3) Preparation
(1) Connection should be made as shown above.
(2) Feed the paper into the printer.
(3) Use a printer designed for MSX. Any printers and plotters can be whichever conform to the Centronics specifications. However, printers not designed for MSX can not print the MSX characters and symbols.
(4) Insert the Test ROM cartridge (facing a label side to you) into the slot.
(5) Keep the cassette tape recorder away from the TV (at least 30 cm ). Since regular cassette tape recorders are for audio use, some are not suitable for the Self Test due to different audio characteristics.
(4) Testing Procedure


|  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { 哥 } \\ & \text { H } \end{aligned}$ |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
| \# |  | m | $\checkmark$ | in |


|  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { 哥 } \\ & \text { H } \end{aligned}$ |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
| \# |  | m | $\checkmark$ | in |


| $\begin{aligned} & \text { 范 } \\ & \text { 最 } \end{aligned}$ |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  | \％ |  |  |
|  |  |  |  |  |  |  |  |
| \％ | $\sigma$ |  | $\bigcirc$ |  | $\exists$ |  |  |




|  | Testing Procedure | CRT Screen displays or Printer prints out | Criteria | Remarks |
| :---: | :---: | :---: | :---: | :---: |
|  | Depress SPACE Key. |  | The overlapped 32 sprites are displayed. <br> If, then, each sprite is moved one by one as shown in the left, it is 0 K . | Sprite check |
|  | Cassette I/0 check Depress SPACE Key. | CRT Screen Displays: | If matched to the left, it is OK. If not, it is NG. | <Important test points> PSG, BUS line CPU-PSG <br> PPI, BUS line CPU-PPI <br> bUS line PPI-Cassette-PSG |




| Step | Testing Procedure | CRT Screen displays or Printer prints out | Criteria | Remarks |
| :---: | :---: | :---: | :---: | :---: |
| 22 | Audio output check <br> Depress SPACE Key. |  <br> Octave 2 Octave 4 Octave 6 When the beep sound is outputted, the corresponding indicator turns red. | If the TV is in the state as the followings, it is OK. <br> 1) "do" in the octave 2 beeps from the channel A, <br> " mi " in it beeps from the channel B , and <br> "so" in it beeps from the channel C . <br> 2) "do" in the octave 4 beeps from the channel <br> A, <br> " mi " in it beeps from the channel B , and <br> "so" in it beeps from the channel C . <br> 3) "do" in the octave 6 beeps from the channel $\stackrel{\text { A }}{\text { " }}$ <br> " m 1 " in it beeps from the channel B , and <br> "so" in it beeps from the channel C . <br> 4) When the beep sound is outputted, the corresponding indicator turns red. | <Important test points> PSG, Sound output circuit, terminals, audio cable, CRT Octave check |
|  |  | CRT Screen Displays: | If the TV is in the state as the followings, it is OK . <br> 1) "do" in the volume 5 beeps from the channel $\stackrel{A}{\mathrm{~A}} \mathrm{~m}$ <br> "mi" in it beeps from the channel B, and <br> "so" in it beeps from the channel C . <br> 2) "do" in the volume 10 beeps from the channel A, <br> " mi " in it beeps from the channel B , and <br> "so" in it beeps from the channel C. <br> 3) "do" in the volume 15 beeps from the channel $\stackrel{\text { A }}{\text { " }}$, <br> "mi" in it beeps from the channel B , and "so" in it beeps from the channel C . <br> 4) When the beep sound is outputted, the corresponding indicator turns red. | Volume check |
|  |  |  <br> NOISE 11 NOISE 21 NOISE 31 When the sound is outputted, the corresponding indicator turns red. | If the TV is in the state as the followings, it <br> is OK . <br> 1) "noise 11 " sound is outputted from the channels $A, B$, and $C$. <br> 2) "noise 21 " sound is outputted from the channels $A, B$, and C. <br> 3) "noise 31 " sound is outputted from the channels A, B, and C. <br> 4) When the sound is outputted, the corresponding indicator turns red. | "Noise" sound check |


| Step | Testing Procedure | CRT Screen displays or Printer prints out | Criteria | Remarks |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | If the TV is in the state as the followings, it is 0 K . <br> 1) When the sound is outputted, the corresponding indicator turns red. <br> 2) The beeps sound like a crossing bell. | Envelope check |
| 23 | Depress SPACE Key. | CRT Screen Displays: <br> Self Test |  |  |
| 24 | Turn off the Printer, TV and Computer. <br> Note: When turning the computer on/off, perform it after turning the printer off. |  |  | Note: Do not turn on the power immediately after turning off the power. <br> Wait at least 30 seconds after turning off the power before turning it back on. |



## Disassembly Instruction



Fig. 28


Fig. 29

| Ref. <br> No. | Procedure | Shown in Fig.- | To remove-. | Remove-. |
| :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | Fig. 28 |  | Screw (3x 6)....... (A) x 3 |
| 2 | 1-2 |  | Top Cabinet | - Cable for the Micro Switches (B) |
| 3 | 1-3 | Fig. 29 |  | Pull the Top Cabinet in the direction of arrow. |

- Note:

1) When disconnecting the cable for the Micro Switches from the Connector CN5, remove it, pressing the top of the Connector.
2) When connecting the cable to the Connector CN5, make sure proper connection. (The lead coloured white must be connected to Pin $l$ of the Connector.)


## Keyboard



| Ref. <br> No. | Procedure | Shown in Fig. - | To remove-. | Remove-. |
| :---: | :---: | :---: | :---: | :---: |
| 4 | 1-5 | Fig. 30 | Keyboard | Screw (3 x 6)........(A) $\times 2$ |
| 5 |  |  |  | Pull the Keyboard in the direction of arrow. |
| 6 | 1-6 | Fig. 31 |  | - Remove the cables of the keyboard from the Connector CN8, CN9. |

- Note: Care should be taken during connection/disconnection of the cable for the Keyboard. With the both sides of the reinforced portion being held, connect/disconnect them.



## Main Board

(A)


Fig. 32 (A)

| Ref. <br> No. | Procedure | Shown in Fig.- | To remove-. | Remove-. |
| :---: | :---: | :---: | :---: | :---: |
| 7 | 1-7 | Fig. 32 | Main Board | Screw (3 x 10) $\qquad$ (A) $\times 5$ <br> Screw (3 x 8) $\qquad$ |
| 8 | 1-3, 8 |  |  | - Remove the Socket from the connector, CN1 and CN2. |
| 9 | 1-9 | Fig. 33 |  | Pull the Main Board in the direction of arrow. |

- Note: When disconnecting the Socket from the Connector CNl, remove it with the latch being pressed.


Connector, CNI

## - Note:

## Video Board

1) When disconnecting the cable from the Connector CN 2 , remove it, pressing the top of the Connector CN2.
2) When connecting the cable to the Connector CN2, make sure proper connection.
(The lead coloured white must be connected to Pin 9 of the Connector.)


Fig. 34


Fig. 35


Fig. 36


| Ref. <br> No. | Procedure | Shown in Fig.- | To remove-. | Remove-. |
| :---: | :---: | :---: | :---: | :---: |
| 10 | 1-11 | Fig. 34 | Shield Plate | Screw (3 x 8)........ (A) $\times 1$ |
| 11 |  |  |  | Pull the Shield Plate in the direction of arrow. |
| 12 | 1-12 | Fig. 35 | Video Board | Screw ( $3 \times 10$ )....... (B) $\times 2$ |
| 13 | 1-13 | Fig. 36 |  | Unlatch the latch of the bottom cabinet. <br> (C) $\times 2$ |
| 14 | 1-14 | Fig. 37 |  | Pull the Video Board in the direction of arrow. |

- Note: When unlatching, avoid applying excessive force to the latch for the rupture.


Power Source Board


Fig. 38

| Ref. <br> No. | Procedure | Shown in Fig.- | To remove-. | Remove-. |
| :---: | :---: | :---: | :---: | :---: |
| 15 | 7-10, 15 | Fig. 38 | Power Source <br> Board | Screw (3x 8)....... (A) $\times 1$ |
| 16 | $7-10,15,16$ |  |  | - Remove the Socket from the Connector, CN101 and CN102. |
| 17 | 7-11, 15-17 |  |  | Pull the Power Source Board in the direction of arrow. |

- Note: When disconnecting the Socket from the Connector, remove it with the latch being pressed.


CN101


CN102



Fig. 40

| Ref. <br> No. | Procedure | Shown in Fig.- | To remove-. | Remove-. |
| :---: | :---: | :---: | :---: | :---: |
| 18 | 1-3, 18, 19 | Fig. 39 | Micro Switches | Screw (3x 10)....... (A) $\times 1$ |
| 19 |  |  |  | Micro Switch......... (B) x 2 |
| 20 | 1-3, 18-20 |  | Slot Panel | - Unlatch the latches of the Slot Panel. <br> (C) $\times 4$ |
| 21 | 1-3, 18-21 | Fig. 40 |  | Remove the Slot Panel in the direction of arrow (1) |
| 22 | 1-3, 18-22 |  | Slot Cover | Remove the Slot Cover in the direction of arrow (2) |

- Note: Care should be taken during disassembly, so as not to damage the slot panel.
When unlatching, avoid applying excessive force to the latch for rupture.



## Adjustment

Channel adjust trimmer

After connecting the TV and computer, turn on the power switch.
Set the TV to UHF channels 35-37. Insert the adjustment screwdriver into the channel adjust trimmer and adjust for a clear picture.

If there is a Spectrul Analyzer, adjustment can be performed precisely. Connect the Spectrul Analyzer to RF output jack of the computer. Then, adjust the channel adjust trimmer as follows.

| Channel | Frequency (MHz) |
| :---: | :---: |
| 35 | 583.25 |
| 36 | 591.25 |
| 37 | 599.25 |



## Power Source

Adjust the VRI so that the DC voltage at Pin 45 of the connector CN7 is within 4.97-5.03 V.


Clock Frequency
Connect the clips of the Frequency counter to the Pin 9 of IC203 on Video Board.
Adjust Trimmer Capacitor, CT201, for $4.43361875 \mathrm{MHz} \pm 3 \mathrm{~Hz}$ reading on Frequency Counter.


## Connector Pin Connection

| General Port 1 and General Port 2 (D-sub 9-pin) |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Signal level TTL level |  |  |  |  |
| Signal Lines List |  |  |  |  |
| Terminal <br> Number | Signal Name | I/0 | (Note 1) | (1) (2) (3) (4) (5) |
| 1 | FWD | I |  |  |
| 2 | BACK | I |  |  |
| 3 | LEFT | I |  | (6) (7) (8) (9) |
| 4 | RIGHT | I |  | ) |
| 5 | +5 V | (Note 2) |  |  |
| 6 | TRG 1 | I/0 | Note 3) | (Front view of the |
| 7 | TRG 2 | I/0 |  | panel-mounted connector) |
| 8 | Output | 0 |  |  |
| 9 | GND | - |  |  |

Note 1: Input or output with respect to the computer
Note 2: Load current 50 mA or less
Note 3: I/O is software controlled. To use an input, set bits 0 and 1 (for port 1) or bits 2 and 3 (for port 2) at PSG port B to high level.

Cassette I/O Port (DIN8-pin)
Signal Lines List

| Terminal <br> Number | Signal <br> Name |
| :---: | :---: |
| 1 | GND |
| 2 | GND |
| 3 | GND |
| 4 | CMTOUT |
| 5 | CMTIN |
| 6 | REM + |
| 7 | REM - |
| 8 | GND |


(Front view of the panel-mounted connector)


Note 1: Input or output with respective to the computer.

Slot 1 and Slot 2
(Card edge type, 50-pin, 2.54 mm pitch)

Signal level TTL level
Signal Lines List (Note 1)

| (Note 1) |  |  |  |  | (Note 1) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Terminal Number | Name | I/0 | Terminal <br> Number | Name | I/0 |
| 1 | $\overline{\text { CS1 }}$ | 0 | 2 | $\overline{\text { CS2 }}$ | 0 |
| 3 | CS12 | 0 | 4 | SLTSL | 0 |
| 5 | (Note 2) | - | 6 | RFSH | 0 |
| 7 | WAIT (Note 3) | I | 8 | INT (Note 3) | I |
| 9 | MI | 0 | 10 | BUSDIR | I |
| 11 | $\overline{\text { IORQ }}$ | 0 | 12 | $\overline{\text { MERQ }}$ | 0 |
| 13 | $\overline{\text { WR }}$ | 0 | 14 | $\overline{\mathrm{RD}}$ | 0 |
| 15 | RESET | 0 | 16 | (Note 2) | - |
| 17 | A9 | 0 | 18 | A15 | 0 |
| 19 | All | 0 | 20 | A10 | 0 |
| 21 | A7 | 0 | 22 | A6 | 0 |
| 23 | Al2 | 0 | 24 | A8 | 0 |
| 25 | Al4 | 0 | 26 | A13 | 0 |
| 27 | A1 | 0 | 28 | A0 | 0 |
| 29 | A3 | 0 | 30 | A2 | 0 |
| 31 | A5 | 0 | 32 | A4 | 0 |
| 33 | D1 | I/0 | 34 | D0 | I/O |
| 35 | D3 | I/0 | 36 | D2 | I/0 |
| 37 | D5 | I/0 | 38 | D4 | I/0 |
| 39 | D7 | I/0 | 40 | D6 | I/0 |
| 41 | GND | - | 42 | CLOCK | 0 |
| 43 | GND | - | 44 | SW1 | - |
| 45 | +5 V (Note 4) | - | 46 | SW2 | _ |
| 47 | +5 V (Note 4) | - | 48 | +12 V (Note 5) | - |
| 49 | SUNDIN | I | 50 | -12 V (Note 6) | - |

Note 1: Input or output with respect to the computer
Note 2: System reserve terminal
Note 3: Be sure to input using an open collector output
Note 4: Load current 300 mA or less
Note 5: Load current 50 mA or less
Note 6: Load current 50 mA or Less
Note 7: Be sure to fully understand the signals before actual
designing a slot connected interface.

Wiring Connection Diagram


## Schematic Diagram (Main Board)




Schematic Diagram (Main Board)


Schematic Diagram (Main Board)


Printed Circuit Board (Main Board)

MICRO SWITCH




## Schematic Diagram (Video Board)



## Printed Circuit Board (Video Board)



## Printed Circuit Board (Keyboard)

Keyboard Matrix



Note: When the Keytop is depressed, contacts of both flexible patterns (, ) contact each other.

## IC Block Diagram

$\qquad$
(1) DN74LS00
(2) DN74LS02
(3) DN74LS04/RVITC74HC04P
(4) DN74LS08
(5) DN74LS09
(6) DN74LS30
(7) DN74LS32
(8) DN74LS74A
(9) DN74LS86
(10) DN74LS107
(11) DN74LS125A
(12) DN74LS138
(13) DN74LS139
(14) DN74LS145
(15) DN74LS153
(16) DN74LS157
(17) DN74LS245
(18) DN74LS273
(19) DN74LS367A
-Others IC
(20) AN2430
(21) AN6553
(22) AN7812R
(23) AN7912T
(24) DA4164ANL12M
(25) DAAY3-8910AG
(26) MN23257CFH
(27) RVITC40H004P
(28) RVITMS9929AJ
(29) UPC311C
(30) UPD416C-3
(31) UPD780C-1
(32) UPD8255AC-5

## EXPlanation of truth tables

The following symbols are now being used in truth tables.
$=$ high level (steady state)
$=$ low level (steady state)
$=$ transition from low to high level
$=$ transition from high to low leve 1
$=$ irrelevant (any input, including transitions)
$=$ off (high-impedance) state of a 3 -state output
a..h $=$ the level of steady-state inputs at inputs A through H respectively
$Q_{0}=1$ evel of $Q$ before the indicated steady-state input conditions were established
$\bar{Q}_{0}=$ complement of $Q_{0}$ or level of $\bar{Q}$ before the indicated
steady-state input conditions were established
$Q_{n}=\begin{aligned} & \text { level of } Q \text { before the most recent active transition } \\ & \text { 1ndicated by } \downarrow \text { or } t\end{aligned}$
$\Omega=$ one high-1evel pulse
= one low-level pulse


| (10) DN74LS107 |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{C C}$ 1CLR 1CK 2 K 2 CLR 2CK 2 J | truth table |  |  |  |  |  |
| [14 13 12 $11 \times 10{ }^{\text {a }}$ | INPUTS |  |  |  | OUTPUTS |  |
| $\xrightarrow{\square}$ | CLR | CLK | $J$ | K | Q | $\overline{\mathrm{Q}}$ |
|  | L | X | X | X | L | H |
|  | H | $\Omega$ | L | L | Q0 | $\bar{Q}_{0}$ |
| $\xrightarrow[\square]{\text { Q Q }}$ | H | $\Omega$ | H | L | H | L |
| 1) | H | $\Omega$ | L | H | L | H |
|  | H | $\Omega$ | H | H |  |  |
| 1J $1 \bar{Q} \quad 1 Q \quad 1 \mathrm{~K}$ | X = irre | evant |  |  |  |  |

(11) DN74LS125A


Positive logic : $Y=A \quad$ Output is off (disabled) when $\overline{\mathrm{OC}}$ is high
(12) DN74LS138



|  | $\begin{aligned} & \text { UTH } \\ & \hline N \end{aligned}$ | PUT | S |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | LEC |  |  |  |  | UTP | UTS |  |  |  |
| $\mathrm{E}_{1}$ | Ex | DC | $\mathrm{DB}^{\text {}}$ | DA | $\overline{\mathrm{Y}}$ | $\bar{Y}$ | $\bar{Y}$ | $\bar{Y}$ | $\mathrm{Y}_{4}$ | Y5 | Y6 | Y |
| X | H | x | x | $\times$ | H | H | H | H | H | H | H | H |
| L | X | x | x | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |
| $\overline{E_{x}}=\bar{E}_{2}+\overline{E_{3}}$ |  |  |  |  |  |  |  |  |  |  |  |  |






-60-

-61-

## Parts Location



Parts Location (Keyboard)


## Packing Instruction



Replacement Parts List
Notes: 1. Parts Name and Location.
Components identified by mark have special characteristics important for safety. When replacing any of these components, use only manufacturer s specified parts.
2. The $S$ mark indicates service standard parts and may differ from production parts.

| Ref. No. | Part No. | Part Name \& Description | $\begin{array}{\|c\|} \hline \text { Per } \\ \text { Set } \\ \hline \end{array}$ | Ref. No. | Part No. | Part Name \& Description | $\begin{array}{\|c\|} \hline \text { Per } \\ \text { Set } \\ \hline \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MAIN P.C. BOARD BLOCK |  |  |  | IC20 | DN74LS00 | IC, QUADRUPLE NAND GATES | 1 |
| IC1 | AN7812R | IC, REGULATOR | 1 | IC21 IC22 | DN74LS125A | IC, RESET BUFFER IC, QUADRUPLE AND GATES | 1 |
| IC2 | AN7912T | IC, REGULATOR | 1 | IC23 | DN74LS139 | IC, DECODER, SLOT | 1 |
| IC3 | DN74LS273 | IC, data latch | 1 | IC24 | DN74LS157 | IC, MULTIPLEXER, DRAM | 1 |
| IC4 | DN74LS32 | IC, QUADRUPLE OR GATES | 1 | IC25 | DN74LS138 | IC, MULTIPLEXER, I/O SELECT | 1 |
| IC5 | DN74LS245 | IC, DATA BUS buFFER | 1 | IC26 | DN74LS367A | IC, ADDRESS CLOCK BUFFER | 1 |
| IC6 | DN74LS74A | IC, RAS |  | IC27 | DN74LS367A | IC, CPU CONTROL BUFFER | 1 |
| IC7 | DN74LS74A | IC, ADRESS CHANGER | , | IC28 | DN74LS157 | IC, MULTIPLEXER, PSG | 1 |
| IC8 | UPD780C-1 | IC, CPU | 1 | IC29 | DN74LS157 | IC, MULTIPLEXER, DRAM | 1 |
| IC9 | DN74LS32 | IC, QUADRUPLE OR GATES |  | IC30 | DN74LS04 | IC, INVERTERS | 1 |
| IC10 | DN74LS153 | IC, DATA SELECTOR, Slot |  | IC31 | DN74LS30 | IC, POSITIVE NAND GATES | 1 |
| ICII | DA4164ANL 12 M | IC, DYNAMIC RAM | 1 | IC32 | MN23257CFH | IC, MASK ROM | 1 |
| IC12 | DA4164ANL12M | IC, DYNAMIC RAM | 1 | IC33 | DN74LS157 | IC, MULTIPLEXER, PSG | 1 |
| IC13 | DA4164ANLI2M | IC, DYNAMIC RAM | 1 | IC34 | AN6553 | IC, OP AMP | 1 |
| IC14 | DA4164ANL12M | IC, DYNAMIC RAM | 1 | IC35 | DN74LS08 | IC, QUADRUPLE AND GATES | 1 |
| IC15 | DA4164ANL12M | IC, DYNAMIC RAM | 1 | IC36 | DAAY3-8910A | IC, PSG (PROGRAMMABLE SOUND | 1 |
| IC16 | DA4164ANL12M | IC, DYNAMIC RAM | 1 |  |  | GENERATOR) |  |
| IC17 | DA4164ANL 12 M | IC, DYNAMIC RAM | 1 | IC37 | DN74LS09 | IC, OPEN COLLECTOR GATES | 1 |
| IC18 | DA4164ANL12M | IC, DYNAMIC RAM | 1 | IC38 | RVITMS9929AJ | IC, VDP (VIDEO display Processor) | 1 |
| IC19 | DN74LS74A | IC, WRITE SIGNaL generator | 1 | IC39 | DN74LS74A | IC, FREQUENCY DIVIDER | 1 |


| Ref. No. | . Part No. | Part Name \& Description | $\begin{array}{\|c\|} \hline \text { Per } \\ \text { Set } \\ \hline \end{array}$ | Ref. No. | Part No. | Part Name \& Description | $\begin{array}{\|c\|} \hline \text { Per } \\ \text { Set } \\ \hline \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IC40 | DN74LS09 | IC, OPEN COLlector gates | 1 | R29 | ERDS2TJ271 | Registor 270 ohms | 1 |
| IC41 | UPC311C | IC, CONPARATOR | 1 | R30 | ERDS2TJ392 | Registor 3.9 K ohms | 1 |
| IC42 | DN74LS74A | IC, FREQUENCY DIVIDER | 1 | R31 | ERDS2TJ471 | Registor 470 ohms | 1 |
| IC43 | RVITC74HC04P | IC, OSCILLATOR | 1 | R32 | ERDS2TJ 220 | Registor 22 ohms | 1 |
| IC44 | DN74LS32 | IC, QUADRUPLE OR GATES | 1 | R33 | ERDS2TJ562 | Registor 5.6 K ohms | 1 |
| IC45 | UPD8255AC-5 | IC, PPI (PROGRAMMABLE PERIPHERAL | 1 | R34 | ERDS2TJ103 | Registor 10K ohms | 1 |
|  |  | INTERFACE) |  | R35 | ERDS2TJ562 | Registor 5.6 K ohms | 1 |
| IC46 | DN74LS145 | IC, KEYBOARD INTERFACE | 1 | R36 | ERDS2TJ681 | Registor 680 ohms | 1 |
| IC47 | DN74LS107 | IC, FREQUENCY DIVIDER | 1 | R37 | ERDS2TJ563 | Registor 56K ohms | 1 |
| IC48 | DN74LS02 | IC, quadruple nor gates | 1 | R38 | ERDS2TJ273 | Registor 27K ohms | 1 |
| IC49 | UPD416C-3 | IC, VIDEO RAM | 1 | R39 | ERDS2TJ220 | Registor 22 ohms | 1 |
| IC50 | UPD416C-3 | IC, VIDEO RAM | 1 | R40 | ERDS2TJ102 | Registor 1K ohms | 1 |
| IC51 | UPD416C-3 | IC, VIDEO RAM | 1 | R41 | ERDS2TJ220 | Registor 22 ohms | 1 |
| IC52 | UPD416C-3 | IC, VIDEO RAM | 1 | R42 | ERDS2TJ220 | Registor 22 ohms | 1 |
| $1 \mathrm{IC53}$ | UPD416C-3 | IC, VIDEO RAM | 1 | R43 | ERDS2TJ472 | Registor 4.7K ohms | 1 |
| IC54 | UPD416C-3 | IC, VIDEO RAM | 1 | R44 | ERDS2TJ220 | Registor 22 ohms | 1 |
| IC55 | UPD416C-3 | IC, VIDEO RAM | 1 | R45 | ERDS2TJ183 | Registor 18 K ohms | 1 |
| IC56 | UPD $416 \mathrm{C}-3$ | IC, VIDEO RAM | 1 | R46 | ERDS2TJ220 | Registor 22 ohms | 1 |
| Q1 | 2SA1061P | Transistor | 1 | R47 | ERDS2TJ220 | Registor 22 ohms | 1 |
| Q2 | 2SA722-S | Transistor | 1 | R48 | ERDS2TJ220 | Registor 22 ohms | 1 |
| Q3 | 2SC829-B | Transistor | 1 | R49 R50 | ERDS2TJ220 | Registor 22 ohms | 1 |
| Q4 | 2SC829-B | Transistor | 1 | R51 | ERDS2TJ220 | Registor 22 ohms Registor 5.6 K ohms | 1 |
| Q5 | $2 \mathrm{SC} 829-\mathrm{B}$ | Transistor | 1 | R52 | ERDS2TJ680 | Registor 5.6 K ohms Registor 68 ohms | 1 |
| Q6 | 2SC1685-Q | Transistor | 1 | R53 | ERDS2TJ103 | Registor Registor 10 K ohms | 1 |
| Q7 | 2SC1318-Q | Transistor | 1 | R54 | ERDS2TJ102 | Registor 1K ohms | 1 |
| Q8 | 2SA722-S | Transistor | 1 | R55 | ERDS2TJ224 | Registor 220 K ohms | 1 |
| Q9 | 2SC1685-Q | Transistor | 1 | R56 | ERDS2TJ222 | Registor 2.2 K ohms | 1 |
| Q10 | 2SC829-B | Transistor | 1 | R57 | ERDS2TJ472 | Registor 4.7K ohms | 1 |
| Q11 | 2SC1685-Q | Transistor | 1 | R58 | ERDS2TJ222 | Registor 2.2 K ohms | 1 |
| D1 | MA165 | Diode | 1 | R59 | ERDS2TJ103 | Registor 10K ohms | 1 |
| D2 | OA91LF | Diode | 1 | R61 | ERDS2TJ105 | Registor 1M ohms | 1 |
| D3 | FBM-032-009 | Diode | 1 | R62 | ERDS2TJ103 | Registor 10K ohms | 1 |
| D4 | FBM-032-009 | Diode | 1 | R63 | ERDS2TJ680 | Registor 68 ohms | 1 |
| D5 | FBM-032-009 | Diode | 1 | R64 | ERD25TJ102 | Registor 1 K ohms | 1 |
| D6 | FBM-032-009 | Diode | 1 | R65 | ERDS2TJ222 | Registor 2.2 K ohms | 1 |
| D7 | DEDS3V20F4 | Diode | 1 | R66 | ERDS2TJ222 | Registor 2.2 K ohms | 1 |
| D8 | DEDS3V20F4 | Diode | 1 | R67 | ERDS2TJ222 | Registor 2.2 K ohms | 1 |
| D9 | MA165 | Diode | 1 | R68 | ERDS2TJ472 | Registor 4.7K ohms | 1 |
| D10 | MA165 | Diode | 1 | R69 | ERDS2TJ223 | Registor 22 K ohms | 1 |
| D11 | MA345B | Diode | 1 | R70 | ERDS2TJ472 | Registor 4.7 K ohms |  |
| D12 | 0A95 | Diode | 1 | R71 | ERDS2TJ472 | Registor 4.7K ohms | 1 |
| D13 | 0A95 | Diode | 1 | R72 | ERDS2TJ182 | Registor 1.8 K ohms | 1 |
| D14 | 0A95 | Diode | 1 | R73 | ERDS2TJ104 | Registor 100K ohms | 1 |
| D15 | MA165 | Diode | 1 | R74 | ERDS2TJ103 | Registor 10K ohms | , |
|  |  |  |  | R75 | ERDS2TJ220 | Registor 22 ohms |  |
| X1 | DECA10678K1M | Crystal | 1 | R76 | ERDS2TJ220 | Registor 22 ohms | 1 |
|  |  |  |  | R77 | ERDS2TJ220 | Registor 22 ohms | 1 |
| RY1 | FBM-450-004 | Relay | 1 | R80 | ERDS2TJ103 | Registor l0K ohms | 1 |
| RA1 | EXBP 87103 J | Component Combination | 1 | $\mathrm{Cl}^{1}$ | ECEAIHV010 | Capacitor $1 \mu \mathrm{~F}$ | 1 |
| RA2 | EXBP87103J | Component Combination | 1 | C2 | ECFF1E1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| RA3 | EXBP88103J | Component Combination | 1 | C3 | ECCFIH680JC | Capacitor 68 pF | 1 |
| RA4 | EXBP 88223J | Component Combination | 1 | C4 | ECCFIH680JC | Capacitor 68 pF | 1 |
|  |  |  |  | C5 | ECCF1H680JC | Capacitor 68 pF | 1 |
| VRI | DENC1B222 | Variable Registor volume | 1 | C6 | ECEAlEU102 | Capacitor $1000 \mu \mathrm{~F}$ | 1 |
|  |  |  |  | C7 | ECEA1CU331 | Capacitor $330 \mu \mathrm{~F}$ | 1 |
| R1 | ERDS2TJ102 | Registor 1K ohms | 1 | C8 | ECQV1H393JZ | Capacitor $0.039 \mu \mathrm{~F}$ | 1 |
| R2 | ERDS2TJ102 | Registor 1K ohms | 1 | C9 | ECQV1H103JZ | Capacitor $0.01 \mu \mathrm{~F}$ | 1 |
| R3 | ERG1SJ680P | Registor 68 ohms | 1 | C10 | ECEALEU472 | Capacitor $4700 \mu \mathrm{~F}$ | 1 |
| R4 | ERDS2TJ472 | Registor 4.7K ohms | 1 | C11 | ECEA1CU682 | Capacitor $6800 \mu \mathrm{~F}$ | 1 |
| R5 | ERDS2TJ153 | Registor 15 K ohms | 1 | C12 | ECEA1CU101 | Capacitor $100 \mu \mathrm{~F}$ | 1 |
| R6 | ERDS2TJ122 | Registor 1.2K ohms | 1 | C13 | ECEA1AU220 | Capacitor $22 \mu \mathrm{~F}$ | 1 |
| R7 | ERDS2TJ122 | Registor 1.2K ohms | 1 | C14 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R8 | ERDS2TJ122 | Registor 1.2K ohms | 1 | C15 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R9 | ERDS2TJ561 | Registor 560 ohms | 1 | C16 | ECFFlE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R10 R11 | ERDS2TJ471 | Registor 470 ohms Registor 4.7 K ohms | 1 | ${ }^{C 17}$ | ECFF1E1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R12 | ERDS2TJ562 | Registor Registor 5.6 K ohms | 1 | C18 | ECEA1AU331 | Capacitor $330 \mu \mathrm{~F}$ Capacitor $100 \mu \mathrm{~F}$ | 1 |
| R13 | ERDS2TJ471 | Registor 470 ohms | 1 | C20 | ECSF1AE 225 | Capacitor 22 HF | 1 |
| R14 | ERDS2TJ561 | Registor 560 ohms | 1 | C21 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R15 | ERDS2TJ471 | Registor 470 ohms | 1 | C22 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R16 | ERDS2TJ561 | Registor 560 ohms | 1 | C23 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R18 | ERDS2TJ101 | Registor 100 ohms | 1 | C24 | ECEALAU101 | Capacitor $100 \mu \mathrm{~F}$ | 1 |
| R19 R20 | ERDS2TJ472 | Registor 4.7 K ohms Registor 2.2 K ohms | 1 | C25 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R21 | ERDS2TJ222 | Registor 2.2K ohms | 1 | C26 | ECFFIE104ZF | $\begin{array}{lll}\text { Capacitor } & 0.1 & \mu \mathrm{~F} \\ \text { Capacitor } & 0.1\end{array}$ | 1 |
| R22 | ERD50TJ151 | Registor 150 ohms | 1 | C28 | ECSF1EE226 | Capacitor $220 \mu \mathrm{~F}$ | 1 |
| R24 | ERG1AN471U | Registor 470 ohms | 1 | C29 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R25 | ERDS2TJ100 | Registor 10 ohms | 1 | C30 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| R26 R27 | ERDS2TJ183 | Registor 18 K ohms Registor 22 ohms | 1 | C31 | ECFF1E104ZF | Capacitor 0.1 <br> Capacitor 2200 <br> F  | 1 |
| R28 | ERDS2TJ562 | Registor 5.6 K ohms | 1 | C32 | ECKD1H222KB | Capacitor 2200 pF | 1 |


| Ref. No. | Part No. | Part Name \& Description | $\begin{aligned} & \text { Per } \\ & \text { Set } \\ & \hline \end{aligned}$ | Ref. No. | Part No. | Part Name \& Description | Per <br> Set |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C33 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | Q203 | 2SC2647B | Transistor | 1 |
| C34 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | Q204 | 2SB6410 | Transistor | 1 |
| C35 | ECKDIH221KB | Capacitor 220 pF |  |  |  |  |  |
| C36 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | D201 | MA165 | Diode | 1 |
| C37 | ECFFIEI04ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | D202 | MA165 | Diode | 1 |
| C38 | ECEALHU3R3 | Capacitor 3.3 $\mu \mathrm{F}$ | 1 | D203 | MA165 | Diode | 1 |
| C39 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | D204 | MA165 | Diode | 1 |
| C40 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | D205 | MA165 | Diode | 1 |
| C41 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |  |  |  |  |
| C42 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | X201 | DECA08867H1M | Crystal | 1 |
| C44 | ECQV1H222J2 | Capacitor $0.0022 \mu \mathrm{~F}$ | 1 |  |  |  |  |
| C45 | ECQVIH104JZ | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | L201 | ELEMY 390KA | Coil | 1 |
| C46 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | L202 | ELEMY 390KA | Coil | 1 |
| C47 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | L203 | ELEMY 390KA | Coil | 1 |
| C48 | ECCDIH330KC | Capacitor 33 pF | 1 | L204 | ELEMY 390KA | Coil | 1 |
| C49 | ECFF1E1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |  |  |  |  |
| C50 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R201 | ERDS2TJ564 | Resistor 560 K ohms | 1 |
| C51 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R202 | ERDS2TJ562 | Resistor 5.6K ohms | 1 |
| C52 | ECSF1AE225 | Capacitor $22 \mu \mathrm{~F}$ | 1 | R203 | ERDS2TJ 101 | Resistor 100 ohms | 1 |
| C53 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R204 | ERDS2TJ102 | Resistor 1K ohms | 1 |
| C54 | ECFF1E1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R205 | ERDS2TJ 393 | Resistor 39 K ohms | 1 |
| C55 | ECSF1AE225 | Capacitor $22 \mu \mathrm{~F}$ | 1 | R206 | ERDS2TJ822 | Resistor 8.2 K ohms | 1 |
| C56 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R207 | ERDS2TJ122 | Resistor 1.2K ohms | 1 |
| C57 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R208 | ERDS2TJ561 | Resistor 560 ohms | 1 |
| C58 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R209 | ERDS2TJ102 | Resistor 1 K ohms | 1 |
| C59 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R210 | ERDS2TJ822 | Resistor 8.2 K ohms | 1 |
| C60 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R211 | ERDS2TJ102 | Resistor 1K ohms | 1 |
| C61 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R212 | ERDS2TJ822 | Resistor 8.2K ohns | 1 |
| C62 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R213 | ERDS2TJ105 | Resistor 1M ohms | 1 |
| C63 | ECFFlE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R215 | ERDS2TJ103 | Resistor 10K ohms | 1 |
| C64 | ECEALCU100 | Capacitor $10 \mu \mathrm{~F}$ | 1 | R216 | ERDS2TJ 393 | Resistor 39K ohms | 1 |
| C65 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R217 | ERDS2TJ103 | Resistor 10 K ohms | 1 |
| C66 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R218 | ERDS2TJ104 | Resistor 100 K ohms | 1 |
| C67 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R219 | ERD25TJ271 | Resistor 270 ohms | 1 |
| C68 | ECCF1H680JC | Capacitor 68 pF | 1 | R220 | ERDS2TJ102 | Resistor 1 K ohms | 1 |
| C69 | ECFF1E104ZF | Capacitor 0.1 $\mu \mathrm{F}$ | 1 | R221 | ERDS2TJ123 | Resistor 12 K ohms | 1 |
| C70 | ECCFIHIS1JC | Capacitor 150 pF | 1 | R222 | ERDS2TJ103 | Resistor 10K ohms | 1 |
| C71 | ECEALAU101 | Capacitor $100 \mu \mathrm{~F}$ | 1 | R223 | ERDS2TJ102 | Resistor 1K ohms | 1 |
| C72 | ECEALAUI01 | Capacitor $100 \mu \mathrm{~F}$ | 1 | R224 | ERDS2TJ471 | Resistor 47 ohms | 1 |
| C73 | ECEA1AU101 | Capacitor $100 \mu \mathrm{~F}$ | 1 | R225 | ERDS2TJ151 | Resistor 150 ohms | 1 |
| C74 | ECEALAU101 | Capacitor $100 \mu \mathrm{~F}$ | 1 | R226 | ERD25TJ221 | Resistor 220 ohms | 1 |
| C75 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R227 | ERDS2TJ680 | Resistor 68 ohms | 1 |
| C76 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R229 | ERDS2TJ102 | Resistor 1 K ohms | 1 |
| C77 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R230 | ERDS2TJ102 | Resistor 1K ohms | 1 |
| C78 | ECFFlE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R231 | ERDS2TJ221 | Resistor 220 ohms | 1 |
| C79 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R232 | ERD25TJ101 | Resistor 100 ohms | 1 |
| C80 | ECFFIE1042F | Capacitor 0.1 $\mu \mathrm{F}$ | 1 | R233 | ERD25TJ102 | Resistor 1 K ohms | 1 |
| C81 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R234 | ERD25TJ272 | Resistor 2.7K ohms | 1 |
| C82 | ECFF1E104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 | R235 | ERD25TJ473 | Resistor 47K ohms | 1 |
| C83 | ECEALCU472 | Capacitor $4700 \mu \mathrm{~F}$ | 1 |  |  |  |  |
| E1 | DFJP5G12 | Connector, CN1 | 1 | Cr201 | ECRH020D11 | Trimmer | 1 |
| E2 | DFJS9H1z | Connector, CN2 | 1 |  |  |  |  |
| E3 | DFJS08J012 | Connector, CN3 | 1 | C201 | ECEAICU100 | Capacitor $10 \mu \mathrm{~F}$ | 1 |
| E4 | FBM-403-075 | Connector, CN4 | 1 | C202 | ECEAICU100 | Capacitor $10 \mu \mathrm{~F}$ | 1 |
| E5 | DFJS 3H1Z | Connector, CN5 | 1 | C203 | ECEALHUR47 | Capacitor $0.47 \mu \mathrm{~F}$ | 1 |
| E6 | EMCAD05001A1 | Connector, CN6, CN7 | 2 | C204 | ECQV1H103JZ | Capacitor $0.01 \mu \mathrm{~F}$ | 1 |
| E7 | DFJS15H1Z | Connector, CN8 | 1 | C205 | ECEA1CU100 | Capacitor $10 \mu \mathrm{~F}$ | 1 |
| E8 | DFJS8H1z | Connector, CN9 | 1 | C206 | ECEALAU470 | Capacitor $47 \mu \mathrm{~F}$ | 1 |
| E9 | FBM-403-052 | Connector, PTl, PT2 | 2 | C207 | ecealau470 | Capacitor $47 \mu \mathrm{~F}$ | 1 |
| E10 | DFUS00012 | Spring | 1 | C208 | ECEAICUIO0 | Capacitor $10 \mu \mathrm{~F}$ | 1 |
| E11 | FBM-415-010 | Fuse Holder | 2 | C209 | ECQVIH103JZ | Capacitor $0.01 \mu \mathrm{~F}$ | 1 |
| E12 | XBAD31501 | Fuse | 1 | C210 | ECEA1HUR47 | Capacitor $0.47 \mu \mathrm{~F}$ | 1 |
| E13 | DFMC00052 | Shield Case, VDP | 1 | C211 | ECCDIH220KC | Capacitor 22 pF | 1 |
| E14 | DFFMY005z | Heat Sink | 1 | C212 | ECCDIH100KC | Capacitor 10 pF | 1 |
| E15 | DFMC00092 | Cover, Shield Case | 4 | C213 | ECCDIH270KC | Capacitor 27 pF | 1 |
| E16 | XSN3+12S | Screw | 4 | C214 | ECCDIH330KC | Capacitor 33 pF | 1 |
| E17 | XWA3B | Washer | 6 | C215 | ECEAICU100 | Capacitor 10 \% | 1 |
| E18 | XNG3ES | Nut | 4 | C216 | ECCFIH330KC | Capacitor 33 pF | 1 |
| E19 | XSN3+10S | Screw | $2$ | C217 | ECEA1CU100 | Capacitor $10 \mu \mathrm{~F}$ | 1 |
| E20 | XWG3 | Washer | 2 | C218 | ECEALCU471 | Capacitor $470 \mu \mathrm{~F}$ | 1 |
| E21 | DDB6M001L-F | Ferrite bead | 9 | C219 | ECFFIE1042F | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| VIDEO P.C.Board Block |  |  |  | C220 | ECEAOJU102 | Capacitor $1000 \mu \mathrm{~F}$ | 1 |
|  |  |  |  | C221 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| IC201 | RVITC4OH004P | IC, OSCILLATOR | 1 | C222 | ECCDIH020KC | Capacitor 2 pF Capacitor 33 pF | 1 |
| IC202 | AN2430 | IC, ENCODER | 1 | C224 | ECEALAUIO1 | Capacitor $100 \mu \mathrm{~F}$ | 1 |
| IC203 | DN74LS74A | IC, FREQUENCY DIVIDER | 1 | C225 | ECEAICU100 | Capacitor $10 \mu \mathrm{~F}$ | 1 |
| IC204 | DN74LS74A | IC, FREQUENCY DIVIDER | 1 | C226 | ECFFIE104ZF | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| IC205 | DN74LS86 | IC, QUADRUPLE OR GATES | 1 |  |  |  |  |
|  |  |  |  | E22 | DFJE0022 | Flat Cable | 1 |
| Q201 | 2SB641Q | Transistor | 1 | E23 | DFUL0005Z | Reinforcement Board | 1 |
| Q202 | 2SC2647B | Transistor | 1 | E24 | DFMC0006Z | Shield Plate | 1 |

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| Ref. No. | Part No. | Part Name \& Description | $\begin{gathered} \hline \text { Per } \\ \text { Set } \end{gathered}$ |
| :---: | :---: | :---: | :---: |
| E25 | DFJF1A001Z | Pin Jack, VIDEO | 1 |
| E26 | DFJF1A002Z | Pin Jack, SOUND | 1 |
| E27 | DFSD0022 | RF Modulater | 1 |
| Power Source Block |  |  |  |
| T101 | DDT5M7E012 | Transformer | 1 |
| 2101 | DDASCO210V | Coil | 1 |
| SW101 | EST15802B | Power Switch | 1 |
| Cl01 | ECQE2A104M | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| C102 | ECQE2A104M | Capacitor $0.1 \mu \mathrm{~F}$ | 1 |
| E28 | DFJP02G12 | Connector, CN101 | 1 |
| E29 | DFJP02G22 | Connector, CN102 | 1 |
| E30 | DFJA03z | AC Cord | 1 |
| E31 | DFJS2G12 | Connector | 1 |
| E32 | DFJT4012 | Contact | 2 |
| E33 | DFUV00032 | Switch Cap | 1 |
| E34 | RHR9932 | Band | 1 |
| E35 | DFMD003Z | Attachment stand | 1 |
| E36 | DFJP02G2Z | Fuse Holder | 2 |
| E37 | XBAD01601 | Fuse | 1 |
| E38 | XTV3+8BFN | Screw | 2 |
| E39 | XTN3+8B | Screw | 4 |
| E40 | XWG3 | Washer | 4 |

Keyboard Block

| D301 | LN220RP | LED, Power | 1 |
| :---: | :---: | :---: | :---: |
| D302 | LN88RCPP | LED, (1) | 1 |
| 1 | DFWV70C0001 | Rey Button F6 F6 | 1 |
| 2 | DFWV70C0002 | Key Button ${ }^{\text {F3 }}{ }^{\text {F2 }} 7$ | 1 |
| 3 | DFWV70C0003 | Key Button ${ }_{\text {F3 }}{ }^{\text {F4 }}$ | 1 |
| 4 | DFWV70C0004 | Key Button F5 F9 | 1 |
| 5 | DFWV70C0005 | Key Button ${ }_{\text {F10 }}$ | 1 |
| 6 | DFWV70C0006 | Key Button STOP | 1 |
| 7 | DFWV70C0007 | Key Button HOME | 1 |
| 8 | DFWV70C0008 | Key Button SELECT | 1 |
| 9 | DFWV70C0009 | Key Button INS | 1 |
| 10 | DFWV70C0010 | Key Button DEL | 1 |
| 11 | DFWV70C0011 | Key Button ESC | 1 |
| 12 | DFWV70C0012 | Key Button ! 1 | 1 |
| 13 | DFWV70C0013 | Key Button © ${ }_{2}$ | 1 |
| 14 | DFWV70C0014 | Key Button \#3 | 1 |
| 15 | DFWV70C0015 | Key Button \$ 4 | 1 |
| 16 | DFWV70C0016 | Key Button \% 5 | 1 |
| 17 | DFWV70C0017 | Key Button * 6 | 1 |
| 18 | DFWV70C0018 | Key Button $\otimes^{7}$ | 1 |
| 19 | DFWV70C0019 | Key Button * 8 | 1 |
| 20 | DFWV70C0020 | Key Button ( 9 | 1 |
| 21 | DFWV70C0021 | Key Button ) ${ }_{0}$ |  |
| 22 | DFWV70C0022 | Key Button = |  |
| 23 | DFWV70C0023 | Key Button $\pm$ | 1 |
| 24 | DFWV70C0024 | Key Button $\overline{\text { \% } /}$ | 1 |
| 25 | DFWV70C0025 | Key Button < | 1 |
| 26 | DFWV70C0026 | Key Button TAB | 1 |
| 27 | DFWV70C0027 | Key Button Q | 1 |
| 28 | DFWV70C0028 | Key Button W | 1 |
| 29 | DFWV70C0029 | Key Button E | 1 |
| 30 | DFWV70C0030 | Key Button R | 1 |
| 31 | DFWV70C0031 | Key Button T | 1 |
| 32 | DFWV70C0032 | Key Button Y | 1 |
| 33 | DFWV70C0033 | Key Button U | 1 |
| 34 | DFWV70C0034 | Key Button I | 1 |
| 35 | DFWV70C0035 | Key Button 0 | 1 |
| 36 | DFWV70C0036 | Key Button P | 1 |
| 37 | DFWV70C0037 | Key Button | 1 |
| 38 | DFWV70C0038 | Key Button | 1 |
| 39 | DFWV70C0039 | Key Button CTRL | 1 |
| 40 | DFWV70C0040 | Key Button A | 1 |
| 41 | DFWV70C0041 | Key Button S |  |
| 42 | DFWV70C0042 | Key Button D | 1 |
| 43 | DFWV70C0043 | Key Button F | 1 |
| 44 | DFWV70C0044 | Key Button G | 1 |
| 45 | DFWV70C0045 | Key Button H | 1 |
| 46 | DFWV70C0046 | Key Button J | 1 |
| 47 | DFWV70C0047 | Key Button K | , |
| 48 | DFWV70C0048 | Key Button L | 1 |


| Ref. No. | Part No. | Part Name \& Description | Per Set |
| :---: | :---: | :---: | :---: |
| 49 | DFWV70C0049 | Key Button ; | 1 |
| 50 | DFWV70C0050 | Key Button '\% | 1 |
| 51 | DFWV70C0051 | Key Button ${ }_{\text {E }}^{\text {E }}$ | 1 |
| 52 | DFWV70C0052 | Key Button | 1 |
| 53 | DFWV70C0053 | Key Button 介 | 1 |
| 54 | DFWV70C0054 | Key Button Z | 1 |
| 55 | DFWV70C0055 | Key Button X | 1 |
| 56 | DFWV70C0056 | Key Button C | 1 |
| 57 | DFWV70C0057 | Key Button V | 1 |
| 58 | DFWV7000058 | Key Button B | 1 |
| 59 | DFWV70C0059 | Key Button N | 1 |
| 60 | DFWV70C0060 | Key Button M | 1 |
| 61 | DFWV7000060 | Key Button , | 1 |
| 62 | DFWV70C0062 | Key Button ? | 1 |
| 63 | DFWV7000063 | Key Button ? | 1 |
| 64 | DFWV70C0064 | Key Button : | 1 |
| 65 | DFWV7000065 | Key Button is | 1 |
| 66 | DFWV7000066 | Key Button (4) | 1 |
| 67 | DFWV70C0067 | Key Button graph | 1 |
| 68 | DFWV70C0068 | Key Button SPACE | 1 |
| 69 | DFWV70C0069 | Key Button CODE | 1 |
| 70 | DFWV70C0070 | Key Button | 1 |
| 71 | DFWV70c0071 | Key Button > | 1 |
| 72 | DFWV70C0072 | Key Button | 1 |
| 73 | DFWV7000073 | Key Button $V$ | 1 |
| E41 | DFWV48A0008 | Flexible Pattern Ass'y | 1 |
| E42 | FBM-652-K20 | Switch Unit A, B, C etc. | 55 |
| E43 | FBM-652-K21 | Switch Unit CURSOR | 4 |
| E44 | FBM-652-K23 | Switch Unit SPACE | 1 |
| E45 | FBM-652-K24 | Switch Unit (4) | 1 |
| E46 | FBM-652-K26 | Switch Unit 0 (left side) | 1 |
| E47 | FBM-652-K25 | Switch Unit | 1 |
| E48 | FBM-652-K22 | Switch Unit FUNCTION | 10 |
| E49 | FBM-652-K22 | Switch Unit SPACE (both ends) | 2 |
| E50 | FBM-717-023 | Arm, SPACE | 1 |
| E51 | FBM-717-022 | Arm, 讴 | 2 |
| E52 | FBM-652-146 | Installation Board, SPACE | 2 |
| E53 | FBM-653-034 | LED Contact | 2 |
| E54 | DFWV65C0005 | LED Holder | 2 |
| Cabinet Block |  |  |  |
| K1 | DFKE00022 | Slot Cover | 2 |
| K2 | FBM-728-011 | Slot Spring | 2 |
| K3 | DFKM00042 | Upper Cabinet | 1 |
| K4 | DFGP00022 | Slot Pannel | 1 |
| K5 | FBM-438-008 | Micro Switch | 2 |
| K6 | DFMD00012 | Pressure Board | 1 |
| K7 | DFDF30012 | Support Shaft | 1 |
| K8 | FBM-845-033 | Connector Cover, CN4 | 1 |
| K9 | DFUV0004Z | Connector Cover, PT1, PT2 | 1 |
| K10 | DFWV80C0006 | Bottom Cabinet Ass'y | 1 |
| K11 | DFMC00042 | RF Shield Plate | 1 |
| K12 | DFMC00032 | Bottom Shield Plate | 1 |
| K13 | DFMY003Z | Heat Sink | 1 |
| K16 | XTN3+10B | Screw | 14 |
| K17 | XWG3 | Washer | 15 |
| K18 | XTV3+16BFZ | Screw | 3 |
| K19 | XTN3+8BFN | Screw | 2 |
| K20 | XTN3+6B | Screw |  |
| K21 | XTN3+6S | Screw | , |
| K22 | XWA3B | Spring Washer |  |
| Accessories |  |  |  |
| K23 | DFJP00Z012 | Cable, CASSETTE | 1 |
| K24 | FBM-497-022 | Cable, SOUND | 1 |
| K25 | DFJPOE012 | Cable, RF | 1 |
| K26 | DFJPOE022 | Cable, VIDEO | 1 |
| K27 | DFPK00212 | Packing Case | 1 |
| K28 | DFPP00012 | Wrap, Set | 1 |
| K29 | DFQA17022 | Graphic Labels | 1 |
| K30 | DFPN0001z | Insulation Material, Right Side | 1 |
| K31 | DFPNOOO22 | Insulation Material, Left Side | , |
| K32 | QPC0072 | AC Cord Cover | 1 |
| K33 | DFQX2004z | BASIC Manual | 1 |
| K34 | DFQX5003Z | Instruction Manual | 1 |

